6GSPS 12 位射频采样模数转换器（ADC）

1 特性

- 分辨率：12-bit , 无失码 (no missing code)
- 采样率：
  CAE2400 : 6 GSPS (单通道) , 3 GSPS (双通道)
- 通道数：1 或 2
- 输入电压范围[$V_{pp,diff}$]：0.8V (typ) , 1V (max)
- 模拟输入带宽(-3dB)： 6 GHz
- 误码率 (Code error rate)： < 10^{-15}
- 积分非线性 INL @ 180 MHz :
  CAE2400 : -2.24 / +1.75 LSB
- 微分非线性 DNL @ 180 MHz :
  CAE2400 : -0.35 / +0.38 LSB
- 信噪比 SNR @ 1.09 GHz , -1 dBFS :
  CAE2400 : 47.3 dBFS ($0.5V_{pp}$) , 50.7 dBFS ($0.8V_{pp}$)
- 无杂散动态范围 SFDR @ 1.09 GHz , -1 dBFS :
  CAE2400 : 68.9 dBc ($0.5V_{pp}$) , 69.4 dBc ($0.8V_{pp}$)
- 有效位 ENOB @ 1.09 GHz , -1 dBFS :
  CAE2400 : 7.5b ($0.5V_{pp}$) , 8.1b ($0.8V_{pp}$)
- 6/12/16 通道 JESD204B 输出，最大通道速率
  16 Gbps，支持 8b/10b 编码，支持
  子类 1 确定性延迟
- 可选数字下变频器(DDC) : 可选滤波
  实数输出支持 1x,2x,3x,4x,6x, 8x,12x,
  16x,24x,32x,48x,64x 抽取比例
  复数输出支持 2x,4x,6x,8x,16x,24x,
  32x, 48x,64x,96x,128x 抽取比例
  每个 DDC 均具有四个独立的 48 位 NCO
  支持快速调频
- 模拟输入通道过压保护
- 片内温度二极管
- 工作温度（结温）: -40 to 115°C
- 低功耗：
  CAE2400 : 2.45W(单通道) , 2.55W (双通道)
- 封装：FCBGA196 (12mm x 12mm)

2 应用

- 示波器和宽带数字转换器
- 宽带通信系统
- 高速数据采集
- 通信测试仪（802.11ad，5G）
- 射频采样软件定义无线电 (SDR)
- 光谱测量

3 概述

CAE2400 是一款 12 位，高速射频采样模数转换器 (ADC)，单通道模式下的最大采样率为 6GSPS，双通道模式下每个通道的最大采样率为 3GSPS。

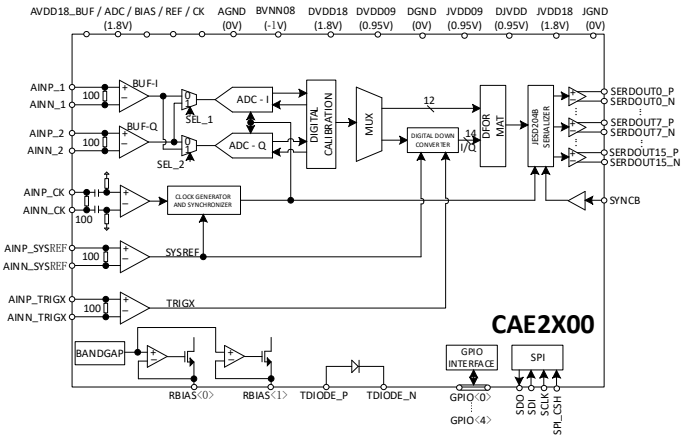
单通道或者双通道工作模式可在线编程配置，可用于开发灵活的硬件，以满足高通道数或宽瞬时信号带宽应用的需求。

CAE2400 采用高速 JESD204B 输出接口，工作温度（结温）支持-40 to 115°C，芯片封装为 FCBGA196 (12mm x 12mm) 。

CAE2400 与 CAE2200/CAE2300/CAE2500/CAE2600/ CAE2700 完全脚位兼容，可根据需求灵活选型。

器件型号	最大采样率 (Gsps)	分辨率 (bits)
CAE2200	10.4(单通道) / 5.2(双通道)	12
CAE2300	8(单通道) / 4(双通道)	12
CAE2400	6(单通道) / 3(双通道)	12
CAE2500	4(单通道) / 2(双通道)	12
CAE2600	2(单通道) / 1(双通道)	12
CAE2700	1(单通道) / 0.5(双通道)	12

4 功能框图



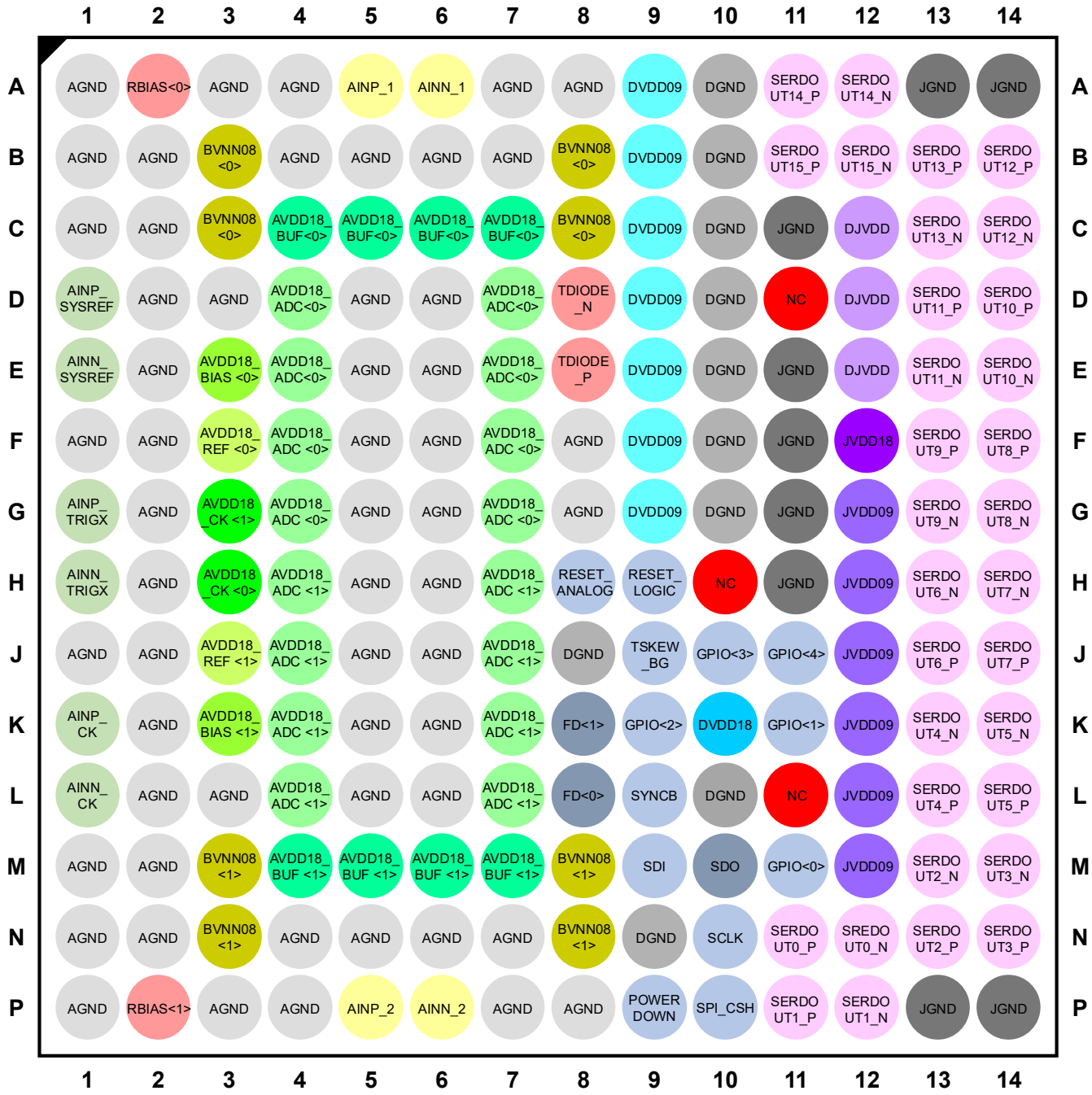
目 录

1 特性 1
2 应用 1
3 概述 1
4 功能框图 1
5 修改历史 3
6 引脚配置和功能描述 (Pin Configuration and Functions) 4
7 技术规格 (Specifications) 8
7.1 电气特性 (Electrical Characteristics) 8
CAE2400 Specifications 8
7.2 时序要求 (Timing Requirements) 14
7.3 典型特性 (Typical Characteristics) 15
8 详细说明 (Detailed Description) 19
8.1 概述 (Overview) 19
8.2 功能框图 (Functional Block Diagram) 19
8.3 信号管脚连接说明 20
8.3.1 模拟信号输入管脚 20
8.3.2 主时钟输入管脚 21
8.3.3 SYSREF 同步信号输入管脚 22
8.3.4 TRIGX 信号输入管脚 22
8.3.5 模拟参考偏置电流管脚 23
8.3.6 温度二极管管脚 23
8.3.7 数字 IO 输入管脚（1.8V 电平） 23
8.3.8 数字 IO 输出管脚（1.8V 电平） 24
8.3.9 JESD204B SerDes 高速输出管脚 24
8.4 电源连接说明 26
8.5 电源滤波电容放置说明 27
9 寄存器说明 (Memory Map) 29
9.1 SPI 控制寄存器说明 29
10 使用说明(Application Information) 69
10.1 初始化设置(Initialization Set Up) 69
10.2 切换单通道/双通道模式 69
10.3 JESD204B 数据映射 70
11 封装尺寸 (Package Outline) 74
12 订购指南 (Orderable Information) 75

5 修改历史

更新日期	版本号	更新内容
2026.9	Rev 2.2	修改 10.1 初始化设置
2026.9	Rev 2.1	更新电气及典型特性数据, 和 10.1 初始化设置
2026.8	Rev 2.0	芯片 pin to pin 升级，模拟输入带宽升级至 6GHz
2026.7	Rev 1.9	10.1 初始化设置流程更新，使用需要注意通过链路状态判断 sysref 是否发生 setup/hold 违例
2026.7	Rev 1.81	10.1 配置 ADC_EN 寄存器值修正为 0x101
2026.4	Rev 1.8	修改了寄存器描述部分，补上所有地址偏移，寄存器统一描述为 32bits 的空间; 寄存器描述后，新增 10 使用说明 (application information)。补充上电后的配置流程，单双通道切换、以及一个 JESD204B 映射示例。
2026.1	Rev 1.7	第 6 章 PinMap 里 AVDD18 以及 JVDD09 电源做了分割。 修改第 9 章寄存器说明，新增了部分控制寄存器。 版面微调。 勘误修正。
2025.11	Rev 1.6	新增 8.3 信号管脚连接说明，8.4 电源连接说明。 新增误码率测试结果。 修改表 6-1 里部分引脚的功能描述。 最高工作温度（结温）从 105°C 调整为 115°C。 寄存器说明调整到 8.5 节。版面调整。
2025.9	Rev 1.4	修改部分性能参数
2025.3	Rev 1.3	寄存器说明增加 APB 读写寄存器, MAC Register, PMA PHY Register
2024.11	Rev 1.2	电气特性 SNR / SINAD / SFDR / ENOB 数据更新。 引脚 P10 的名称由 CONVST 改为 SPI_CSH。勘误修正
2024.11	Rev 1.1	增加寄存器说明
2024.10	Rev 1.0	
2024.5	Rev PreB	初版

6 引脚配置和功能描述 (Pin Configuration and Functions)



Top View

Not to scale

图 6-1. 196-Ball Flip Chip BGA

表 6-1. 引脚功能 (Pin Functions)

管脚序号	管脚名	类型	功能描述
A2 P2	RBIAS<0> RBIAS<1>	输入	每个管脚接 12k 电阻到地。用于产生模拟电路内部参考电流。 注意 12k 电阻必须是高精度低温票电阻(建议采用 0.1%精度，温漂小于 25ppm/ºC)
A5	AINP_1	输入	双通道模式：第一模拟通道差分输入的正输入（I-channel） 单通道模式：默认模拟通道差分输入的正输入（I 或者 Q channel） 它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。 默认状态下为单通道模式的模拟输入接口。
A6	AINN_1	输入	双通道模式：第一模拟通道差分输入的负输入（I-channel） 单通道模式：默认模拟通道差分输入的负输入（I 或者 Q channel） 它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。 默认状态下为单通道模式的模拟输入接口。
P5	AINP_2	输入	双通道模式：第二模拟通道差分输入的正输入（Q-channel） 单通道模式：可选模拟通道差分输入的正输入（I 或者 Q channel） 它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。 需要通过 SPI 才能切换为单通道模式的模拟输入接口。
P6	AINN_2	输入	双通道模式：第二模拟通道差分输入的负输入（Q-channel） 单通道模式：可选模拟通道差分输入的负输入（I 或者 Q channel） 它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。 需要通过 SPI 才能切换为单通道模式的模拟输入接口。
D1	AINP_SYSREF	输入	SYSREF 差分输入信号（正端），用于同步多 ADC 芯片数据时序给 FGPA。它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。
E1	AINN_SYSREF	输入	SYSREF 差分输入信号（负端），用于同步多 ADC 芯片数据时序给 FGPA。它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。
G1	AINP_TRIGX	输入	触发器(Trigger) X 差分信号(正端)，用于 DDC 模块的频率跳变。它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。
H1	AINN_TRIGX	输入	触发器(Trigger) X 差分信号(负端)，用于 DDC 模块的频率跳变。它内接 50 欧姆电阻，支持 DC 或者 AC 耦合。请注意，该管脚必须满足输入共模电压范围及摆幅的要求。
K1	AINP_CK	输入	主时钟差分信号(正端)，该管脚给芯片提供主时钟，芯片内部通过 50 欧姆电阻 AC 耦合，但该管脚必须满足输入共模电压范围及摆幅的要求。
L1	AINN_CK	输入	主时钟差分信号(负端)，该管脚给芯片提供主时钟， 芯片内部通过 50 欧姆电阻 AC 耦合，但该管脚必须满足输入共模电压范围及摆幅的要求。
E8	TDIODE_P	输入	温度二极管正（阳极）连接，通过外置温度传感器来监视芯片结温. 该管脚没被使用时，请悬空。
D8	TDIODE_N	输入	温度二极管负（阴极）连接，通过外置温度传感器来监视芯片结温. 该管脚没被使用时，请悬空。
B3, B8, C3, C8 M3, M8, N3, N8	BVNN08<0> BVNN08<1>	输入	模拟电路负电源供电管脚。它们连接到外部负 LDO 电源，该电源必须满足规范中的负电位和漏电流要求。
C4, C5, C6, C7 M4,M5, M6, M7	AVDD18_BUF<0> AVDD18_BUF<1>	输入	1.8V 模拟输入 Buffer 电源

表 6-1. 引脚功能 (续)

管脚序号	管脚名	类型	功能描述
E3 K3	AVDD18_BIAS<0> AVDD18_BIAS<1>	输入	1.8V 模拟 BIAS 电源
D4, D7, E4, E7, F4, F7, G4, G7 H4, H7, J4, J7, K4, K7, L4, L7	AVDD18_ADC<0> AVDD18_ADC<1>	输入	1.8V 模拟 ADC 电源
F3 J3	AVDD18_REF<0> AVDD18_REF<1>	输入	1.8V 模拟 REF 电源
H3 G3	AVDD18_CK<0> AVDD18_CK<1>	输入	1.8V 模拟时钟电源
A1, A3, A4, A7, A8, B1, B2, B4, B5, B6, B7, C1, C2, D2, D3, D5, D6, E2, E5, E6, F1, F2, F5, F6, F8, G2, G5, G6, G8, H2, H5, H6, J1, J2, J5, J6, K2, K5, K6, L2, L3, L5, L6, M1, M2, N1, N2, N4, N5, N6, N7, P1, P3, P4, P7, P8	AGND	输入	模拟地
A9, B9, C9, D9, E9, F9, G9	DVDD09	输入	0.95V 数字内核电源
K10	DVDD18	输入	1.8V 数字接口电源
A10, B10, C10, D10, E10, F10, J8, N9, G10, L10,	DGND	输入	数字地
H8	RESET_ANALOG	输入	模拟电路复位管脚。一旦提供了主时钟，该管脚对时钟产生器进行复位。高电平时复位，正常工作时保持低电平，1.8V 逻辑。
H9	RESET_LOGIC	输入	数字电路复位管脚。高电平时复位，正常工作时请保持低电平。 芯片上电时，芯片内部的 POR 电路会复位所有的数字电路，此时该复位信号可以忽略，1.8V 逻辑。
L8 K8	FD<0> FD<1>	输出	信号饱和快速检测管脚， FD<0> 对应 I-channel，FD<1> 对应 Q-channel，1.8V 逻辑。
J11 J0 K9 K11 M11	GPIO<4> GPIO<3> GPIO<2> GPIO<1> GPIO<0>	输入	用于 DDC 的快速频率跳转。1.8V 逻辑。
J9	TSKEW_BG	输入	该管脚为高电平时可以启动后台时序偏差校准（background timing skew calibration），1.8V 逻辑。
L9	SYNCB	输入	JESD204B 同步信号。低电平时，JESD204B 与接收器正进行握手，握手完成后，该管脚转为高电平，1.8V 逻辑。
P10	SPI_CSH	输入	SPI 片选使能信号， 0 将复位 SPI，当 SPI 进行读写时，保持为 1，1.8V 逻辑。

表 6-1. 引脚功能 (续)

管脚序号	管脚名	类型	功能描述
N10	SCLK	输入	SPI 时钟信号，1.8V 逻辑。
M9	SDI	输入	SPI 输入信号，1.8V 逻辑。
M10	SDO	输出	SPI 输出信号，1.8V 逻辑。
P9	POWERDOWN	输入	芯片断电模式管脚，输入高电平将芯片断电，正常工作时保持低电平，1.8V 逻辑。
D11, H10, L11	NC	/	悬空，不连接。NC 引脚禁止接地或接高电平处理。
C12, D12, E12	DJVDD	输入	0.95V JESD204B 数字内核供电
G12, H12, J12, K12, L12, M12	JVDD09	输入	0.95V JESD204B SerDes 接口供电
F12	JVDD18	输入	1.8V JESD204B 接口 I/O 供电
A13, A14, C11, E11, F11, G11, H11, P13, P14	JGND	输入	JESD204B 接口地
N11 N12	SERDOUT0_P SERDOUT0_N	输出	Lane 0 差分 SerDes 输出对，内接 100 欧姆电阻
P11 P12	SERDOUT1_P SERDOUT1_N	输出	Lane 1 差分 SerDes 输出对，内接 100 欧姆电阻
N13 M13	SERDOUT2_P SERDOUT2_N	输出	Lane 2 差分 SerDes 输出对，内接 100 欧姆电阻
N14 M14	SERDOUT3_P SERDOUT3_N	输出	Lane 3 差分 SerDes 输出对，内接 100 欧姆电阻
L13 K13	SERDOUT4_P SERDOUT4_N	输出	Lane 4 差分 SerDes 输出对，内接 100 欧姆电阻
L14 K14	SERDOUT5_P SERDOUT5_N	输出	Lane 5 差分 SerDes 输出对，内接 100 欧姆电阻
J13 H13	SERDOUT6_P SERDOUT6_N	输出	Lane 6 差分 SerDes 输出对，内接 100 欧姆电阻
J14 H14	SERDOUT7_P SERDOUT7_N	输出	Lane 7 差分 SerDes 输出对，内接 100 欧姆电阻
F14 G14	SERDOUT8_P SERDOUT8_N	输出	Lane 8 差分 SerDes 输出对，内接 100 欧姆电阻
F13 G13	SERDOUT9_P SERDOUT9_N	输出	Lane 9 差分 SerDes 输出对，内接 100 欧姆电阻
D14 E14	SERDOUT10_P SERDOUT10_N	输出	Lane 10 差分 SerDes 输出对，内接 100 欧姆电阻
D13 E13	SERDOUT11_P SERDOUT11_N	输出	Lane 11 差分 SerDes 输出对，内接 100 欧姆电阻
B14 C14	SERDOUT12_P SERDOUT12_N	输出	Lane 12 差分 SerDes 输出对，内接 100 欧姆电阻
B13 C13	SERDOUT13_P SERDOUT13_N	输出	Lane 13 差分 SerDes 输出对，内接 100 欧姆电阻
A11 A12	SERDOUT14_P SERDOUT14_N	输出	Lane 14 差分 SerDes 输出对，内接 100 欧姆电阻
B11 B12	SERDOUT15_P SERDOUT15_N	输出	Lane 15 差分 SerDes 输出对，内接 100 欧姆电阻

7 技术规格 (Specifications)

7.1 电气特性 (Electrical Characteristics)

CAE2400 Specifications

Parameter	Conditions	CAE2400			Unit
		Min	Typ	Max	
Analog Input					
Full-scale input range	Fully differential	0.5	0.8	1.0	Vpp,diff
Input Termination	Single-ended to AGND		50		Ω
	Differential		100		Ω
Single Input capacitance	Single-ended to AGND		400		fF
Differential Input capacitance	Differential inputs		80		fF
Input Common Mode	$V_{CM,input}$	0.40	0.45	0.50	V
Input Signal Bandwidth	-3dB bandwidth		6		GHz
SerDes Output					
Differential Output Voltage	Normal mode	0.45		0.50	Vpp,diff
Output Common Mode Voltage	AC coupled	0.57	0.63	0.79	V
Output Termination	Differential		100		Ω
Clock Input					
Differential Input Voltage	100 ohm differential, on-chip	0.3	1	2	Vpp,diff
Input Common Mode Voltage	$V_{CM,CLKIN}$	0.2	0.3	0.4	V
Clock Frequency	F_{CLK}			3.0	GHz
Duty Cycle			50.0		%
Single Input Capacitance	Single-ended to AGND		400		fF
Differential Input Capacitance	Differential inputs		80		fF
SYSREF Input					
Differential Input Voltage	100 ohm differential, on-chip	0.5	1.0	2.0	Vpp,diff
Input Common Mode Voltage	$V_{CM,SYSREFIN}$		0.9		V
Frequency	Periodic mode		18.75	46.875	MHz
Pulse Width	Burst and Periodic modes	333.33			ps
Single Input Capacitance	Single-ended to AGND		450		fF
Differential Input Capacitance	Differential inputs		90		fF
Reference Voltage					
Internal Reference Voltage	Fully Differential	±0.39	±0.4	±0.41	V
Tempco	From -40°C to 125°C		±50	±100	ppm/°C
DC Accuracy					
Resolution	DC code		12		bit
INL	Best-Fit		±2.2		LSB
DNL	(no missing code)		±0.38		LSB
Offset Error	DC code error		±3		mV
Code Error Rate	Whole chip		$< 10^{-15}$		Error/ samples

CAE2400 Specifications (Continued)

Parameter	Conditions *Single-Channel Mode , 6 GSPS*	CAE2400			Unit
		Min	Typ	Max	
AC Accuracy					
SNR	Fin = 180MHz, -1.0 dBFS (0.5Vpp FS)		47.6		dBFS
	Fin = 180MHz, -10.0 dBFS (0.5Vpp FS)		47.7		
	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		51.4		dBFS
	Fin = 180MHz, -10.0 dBFS (0.8Vpp FS)		51.5		
	Fin = 1.09GHz, -1.0 dBFS (0.5Vpp FS)		47.3		dBFS
	Fin = 1.09GHz, -10.0 dBFS (0.5Vpp FS)		47.6		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		50.7		dBFS
	Fin = 1.09GHz, -10.0 dBFS (0.8Vpp FS)		51.4		
	Fin = 1.9GHz, -1.0 dBFS (0.5Vpp FS)		46.5		dBFS
	Fin = 1.9GHz, -10.0 dBFS (0.5Vpp FS)		47.6		
	Fin = 1.9GHz, -1.0 dBFS (0.8Vpp FS)		49.5		dBFS
	Fin = 1.9GHz, -10.0 dBFS (0.8Vpp FS)		51.4		
	Fin = 2.9GHz, -1.0 dBFS (0.5Vpp FS)		45.2		dBFS
	Fin = 2.9GHz, -10.0 dBFS (0.5Vpp FS)		47.3		
	Fin = 2.9GHz, -1.0 dBFS (0.8Vpp FS)		47.1		dBFS
	Fin = 2.9GHz, -10.0 dBFS (0.8Vpp FS)		50.8		
	Fin = 3.9GHz, -1.0 dBFS (0.5Vpp FS)		44.1		dBFS
	Fin = 3.9GHz, -10.0 dBFS (0.5Vpp FS)		47.0		
	Fin = 3.9GHz, -1.0 dBFS (0.8Vpp FS)		45.0		dBFS
	Fin = 3.9GHz, -10.0 dBFS (0.8Vpp FS)		50.3		
	Fin = 4.9GHz, -1.0 dBFS (0.5Vpp FS)		42.9		dBFS
	Fin = 4.9GHz, -10.0 dBFS (0.5Vpp FS)		46.7		
	Fin = 4.9GHz, -1.0 dBFS (0.8Vpp FS)		43.2		dBFS
	Fin = 4.9GHz, -10.0 dBFS (0.8Vpp FS)		49.8		
SINAD	Fin = 180MHz, -1.0 dBFS (0.5Vpp FS)		47.5		dBFS
	Fin = 180MHz, -10.0 dBFS (0.5Vpp FS)		47.5		
	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		51.1		dBFS
	Fin = 180MHz, -10.0 dBFS (0.8Vpp FS)		51.1		
	Fin = 1.09GHz, -1.0 dBFS (0.5Vpp FS)		47.2		dBFS
	Fin = 1.09GHz, -10.0 dBFS (0.5Vpp FS)		47.5		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		50.5		dBFS
	Fin = 1.09GHz, -10.0 dBFS (0.8Vpp FS)		51.1		
	Fin = 1.9GHz, -1.0 dBFS (0.5Vpp FS)		46.2		dBFS
	Fin = 1.9GHz, -10.0 dBFS (0.5Vpp FS)		47.4		
	Fin = 1.9GHz, -1.0 dBFS (0.8Vpp FS)		48.9		dBFS
	Fin = 1.9GHz, -10.0 dBFS (0.8Vpp FS)		50.9		
	Fin = 2.9GHz, -1.0 dBFS (0.5Vpp FS)		45.1		dBFS
	Fin = 2.9GHz, -10.0 dBFS (0.5Vpp FS)		47.2		
	Fin = 2.9GHz, -1.0 dBFS (0.8Vpp FS)		46.6		dBFS
	Fin = 2.9GHz, -10.0 dBFS (0.8Vpp FS)		50.4		

CAE2400 Specifications (Continued)

Parameter	Conditions *Single-Channel Mode , 6 GSPS*	CAE2400			Unit
		Min	Typ	Max	
AC Accuracy					
SINAD	Fin = 3.9GHz, -1.0 dBFS (0.5Vpp FS)		43.9		dBFS
	Fin = 3.9GHz, -10.0 dBFS (0.5Vpp FS)		46.8		
	Fin = 3.9GHz, -1.0 dBFS (0.8Vpp FS)		44.7		dBFS
	Fin = 3.9GHz, -10.0 dBFS (0.8Vpp FS)		49.8		
	Fin = 4.9GHz, -1.0 dBFS (0.5Vpp FS)		42.8		dBFS
	Fin = 4.9GHz, -10.0 dBFS (0.5Vpp FS)		46.6		
	Fin = 4.9GHz, -1.0 dBFS (0.8Vpp FS)		42.8		dBFS
	Fin = 4.9GHz, -10.0 dBFS (0.8Vpp FS)		49.4		
SFDR	Fin = 180MHz, -1.0 dBFS (0.5Vpp FS)		68.3		dBc
	Fin = 180MHz, -10.0 dBFS (0.5Vpp FS)		64.5		
	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		68.6		dBc
	Fin = 180MHz, -10.0 dBFS (0.8Vpp FS)		63.2		
	Fin = 1.09GHz, -1.0 dBFS (0.5Vpp FS)		68.9		dBc
	Fin = 1.09GHz, -10.0 dBFS (0.5Vpp FS)		66.1		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		69.4		dBc
	Fin = 1.09GHz, -10.0 dBFS (0.8Vpp FS)		64.1		
	Fin = 1.9GHz, -1.0 dBFS (0.5Vpp FS)		62.7		dBc
	Fin = 1.9GHz, -10.0 dBFS (0.5Vpp FS)		61.4		
	Fin = 1.9GHz, -1.0 dBFS (0.8Vpp FS)		60.8		dBc
	Fin = 1.9GHz, -10.0 dBFS (0.8Vpp FS)		61.1		
	Fin = 2.9GHz, -1.0 dBFS (0.5Vpp FS)		61.7		dBc
	Fin = 2.9GHz, -10.0 dBFS (0.5Vpp FS)		63.4		
	Fin = 2.9GHz, -1.0 dBFS (0.8Vpp FS)		58.2		dBc
	Fin = 2.9GHz, -10.0 dBFS (0.8Vpp FS)		62.5		
	Fin = 3.9GHz, -1.0 dBFS (0.5Vpp FS)		59.3		dBc
	Fin = 3.9GHz, -10.0 dBFS (0.5Vpp FS)		62.6		
	Fin = 3.9GHz, -1.0 dBFS (0.8Vpp FS)		58.5		dBc
	Fin = 3.9GHz, -10.0 dBFS (0.8Vpp FS)		61.4		
	Fin = 4.9GHz, -1.0 dBFS (0.5Vpp FS)		57.9		dBc
	Fin = 4.9GHz, -10.0 dBFS (0.5Vpp FS)		62.9		
	Fin = 4.9GHz, -1.0 dBFS (0.8Vpp FS)		55.5		dBc
	Fin = 4.9GHz, -10.0 dBFS (0.8Vpp FS)		61.7		

CAE2400 Specifications (Continued)

Parameter	Conditions *Single-Channel Mode , 6 GSPS*	CAE2400			Unit
		Min	Typ	Max	
AC Accuracy					
HD2	Fin = 180MHz, -1.0 dBFS (0.5Vpp FS)		-82.1		dBFS
	Fin = 180MHz, -10.0 dBFS (0.5Vpp FS)		-73.2		
	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		-82.0		dBFS
	Fin = 180MHz, -10.0 dBFS (0.8Vpp FS)		-78.4		
	Fin = 1.09GHz, -1.0 dBFS (0.5Vpp FS)		-80.5		dBFS
	Fin = 1.09GHz, -10.0 dBFS (0.5Vpp FS)		-77.7		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		-83.1		dBFS
	Fin = 1.09GHz, -10.0 dBFS (0.8Vpp FS)		-83.1		
	Fin = 1.9GHz, -1.0 dBFS (0.5Vpp FS)		-67.3		dBFS
	Fin = 1.9GHz, -10.0 dBFS (0.5Vpp FS)		-74.9		
	Fin = 1.9GHz, -1.0 dBFS (0.8Vpp FS)		-64.8		dBFS
	Fin = 1.9GHz, -10.0 dBFS (0.8Vpp FS)		-78.1		
	Fin = 2.9GHz, -1.0 dBFS (0.5Vpp FS)		-64.5		dBFS
	Fin = 2.9GHz, -10.0 dBFS (0.5Vpp FS)		-75.8		
	Fin = 2.9GHz, -1.0 dBFS (0.8Vpp FS)		-60.4		dBFS
	Fin = 2.9GHz, -10.0 dBFS (0.8Vpp FS)		-76.0		
	Fin = 3.9GHz, -1.0 dBFS (0.5Vpp FS)		-68.5		dBFS
	Fin = 3.9GHz, -10.0 dBFS (0.5Vpp FS)		-73.3		
	Fin = 3.9GHz, -1.0 dBFS (0.8Vpp FS)		-63.7		dBFS
	Fin = 3.9GHz, -10.0 dBFS (0.8Vpp FS)		-73.6		
	Fin = 4.9GHz, -1.0 dBFS (0.5Vpp FS)		-62.8		dBFS
	Fin = 4.9GHz, -10.0 dBFS (0.5Vpp FS)		-80.6		
	Fin = 4.9GHz, -1.0 dBFS (0.8Vpp FS)		-57.7		dBFS
	Fin = 4.9GHz, -10.0 dBFS (0.8Vpp FS)		-76.1		
HD3	Fin = 180MHz, -1.0 dBFS (0.5Vpp FS)		-68.3		dBFS
	Fin = 180MHz, -10.0 dBFS (0.5Vpp FS)		-64.4		
	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		-68.6		dBFS
	Fin = 180MHz, -10.0 dBFS (0.8Vpp FS)		-63.2		
	Fin = 1.09GHz, -1.0 dBFS (0.5Vpp FS)		-76.3		dBFS
	Fin = 1.09GHz, -10.0 dBFS (0.5Vpp FS)		-65.9		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		-83.9		dBFS
	Fin = 1.09GHz, -10.0 dBFS (0.8Vpp FS)		-64.2		
	Fin = 1.9GHz, -1.0 dBFS (0.5Vpp FS)		-62.7		dBFS
	Fin = 1.9GHz, -10.0 dBFS (0.5Vpp FS)		-61.3		
	Fin = 1.9GHz, -1.0 dBFS (0.8Vpp FS)		-60.8		dBFS
	Fin = 1.9GHz, -10.0 dBFS (0.8Vpp FS)		-61.1		
	Fin = 2.9GHz, -1.0 dBFS (0.5Vpp FS)		-61.8		dBFS
	Fin = 2.9GHz, -10.0 dBFS (0.5Vpp FS)		-63.4		
	Fin = 2.9GHz, -1.0 dBFS (0.8Vpp FS)		-58.3		dBFS
	Fin = 2.9GHz, -10.0 dBFS (0.8Vpp FS)		-62.5		

CAE2400 Specifications (Continued)

Parameter	Conditions *Single-Channel Mode , 6 GSPS*	CAE2400			Unit
		Min	Typ	Max	
AC Accuracy					
HD3	Fin = 3.9GHz, -1.0 dBFS (0.5Vpp FS)		-64.0		dBFS
	Fin = 3.9GHz, -10.0 dBFS (0.5Vpp FS)		-62.6		
	Fin = 3.9GHz, -1.0 dBFS (0.8Vpp FS)		-62.3		dBFS
	Fin = 3.9GHz, -10.0 dBFS (0.8Vpp FS)		-61.3		
	Fin = 4.9GHz, -1.0 dBFS (0.5Vpp FS)		-60.5		dBFS
	Fin = 4.9GHz, -10.0 dBFS (0.5Vpp FS)		-63.0		
	Fin = 4.9GHz, -1.0 dBFS (0.8Vpp FS)		-57.7		dBFS
	Fin = 4.9GHz, -10.0 dBFS (0.8Vpp FS)		-61.6		
ENOB	Fin = 180MHz, -1.0 dBFS (0.5Vpp FS)		7.6		Bit
	Fin = 180MHz, -10.0 dBFS (0.5Vpp FS)		7.6		
	Fin = 180MHz, -1.0 dBFS (0.8Vpp FS)		8.2		Bit
	Fin = 180MHz, -10.0 dBFS (0.8Vpp FS)		8.2		
	Fin = 1.09GHz, -1.0 dBFS (0.5Vpp FS)		7.5		Bit
	Fin = 1.09GHz, -10.0 dBFS (0.5Vpp FS)		7.6		
	Fin = 1.09GHz, -1.0 dBFS (0.8Vpp FS)		8.1		Bit
	Fin = 1.09GHz, -10.0 dBFS (0.8Vpp FS)		8.2		
	Fin = 1.9GHz, -1.0 dBFS (0.5Vpp FS)		7.4		Bit
	Fin = 1.9GHz, -10.0 dBFS (0.5Vpp FS)		7.6		
	Fin = 1.9GHz, -1.0 dBFS (0.8Vpp FS)		7.8		Bit
	Fin = 1.9GHz, -10.0 dBFS (0.8Vpp FS)		8.2		
	Fin = 2.9GHz, -1.0 dBFS (0.5Vpp FS)		7.2		Bit
	Fin = 2.9GHz, -10.0 dBFS (0.5Vpp FS)		7.5		
	Fin = 2.9GHz, -1.0 dBFS (0.8Vpp FS)		7.4		Bit
	Fin = 2.9GHz, -10.0 dBFS (0.8Vpp FS)		8.1		
	Fin = 3.9GHz, -1.0 dBFS (0.5Vpp FS)		7.0		Bit
	Fin = 3.9GHz, -10.0 dBFS (0.5Vpp FS)		7.5		
	Fin = 3.9GHz, -1.0 dBFS (0.8Vpp FS)		7.1		Bit
	Fin = 3.9GHz, -10.0 dBFS (0.8Vpp FS)		8.0		
	Fin = 4.9GHz, -1.0 dBFS (0.5Vpp FS)		6.8		Bit
	Fin = 4.9GHz, -10.0 dBFS (0.5Vpp FS)		7.4		
	Fin = 4.9GHz, -1.0 dBFS (0.8Vpp FS)		6.8		Bit
	Fin = 4.9GHz, -10.0 dBFS (0.8Vpp FS)		7.9		

CAE2400 Specifications (Continued)

Parameter	Conditions	CAE2400			Unit
		Min	Typ	Max	
AC Accuracy					
Noise Floor Density	At 180MHz, -10 dBFS (0.8Vpp FS)		-146.3		dBFS/√Hz
Speed					
ADC Sampling rate	Single-channel		6.0		GSPS
	Dual-Channel		3.0		GSPS
JESD204B lane rate	SerDes lane rate, 100 ohm termination	1.25	7.5	15.0	Gbps
Power Supplies					
AVDD18_BUF , AVDD18_ADC , AVDD18_BIAS , AVDD18_REF , AVDD18_CK , DVDD18 , JVDD18	1.8V power supplies	1.7	1.8	1.9	V
DVDD09 , JVDD09 , DJVDD	0.95V power supplies	0.9	0.95	0.975	V
BVNN08	Analog negative power supplies	-0.95	-1.0	-1.05	V
Current (1.8V supplies)	Normal mode, all background calibrations enable & DDC off (single)		1000		mA
	Normal mode, all background calibrations enable & DDC off (dual)		1072		
Current (0.95V supplies)	Normal mode, all background calibrations enable & DDC off		650		mA
Current (1.8V supplies)	Power down		26		mA
Current (0.95V supplies)	Power down		10		mA
Power Consumption	Normal mode, all background calibrations enable & DDC off (single)		2.45		W
	Normal mode, all background calibrations enable & DDC off (dual)		2.55		
Junction Temperature	T_{MIN} to T_{MAX}	-40		115	°C
Long-Term Reliability	For Pro-longed use	-40		105	°C

7.2 时序要求 (Timing Requirements)

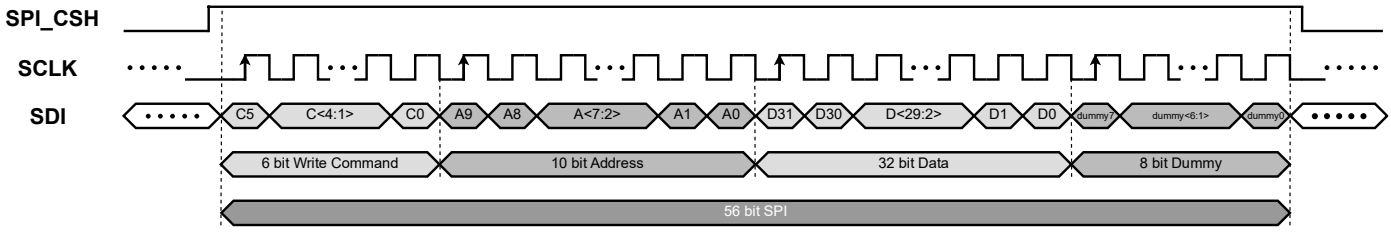


图 7-1. SPI 写数据接口波形

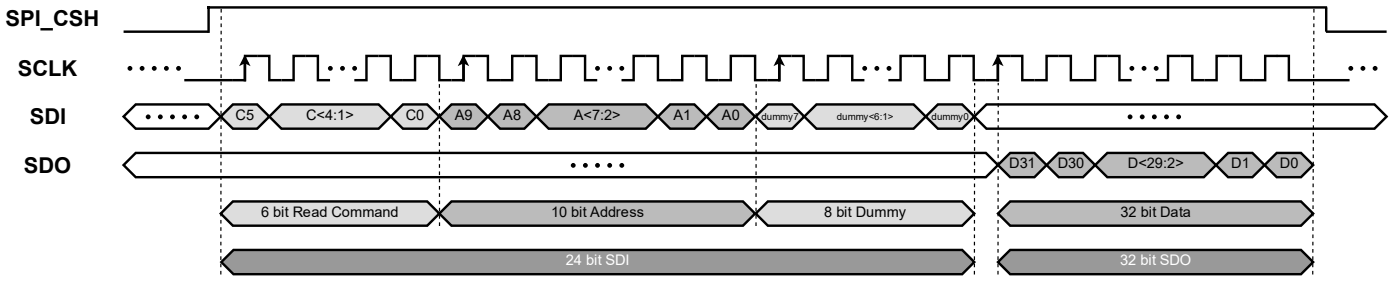


图 7-2. SPI 读数据接口波形

寄存器 SPI 读写：

芯片复位后 SPI 读写寄存器，相关的信号 SPI_CSH 默认为 1。

SPI 读写寄存器需要 56bits。6 位命令字+ 10 位为地址+40 位数据。
6 位命令字的控制为 6b0001_00 写寄存器，6b0010_00 读寄存器。

以 SPI 写 SPI 第一寄存器 32'h14183102 为例，spi_wr_reg(10'h001,32'h14183102) 测试 pattern 波形：
前面 6 个 SCLK， 对应 SDI 为 6b0001_00，所以是 SPI 写。后面 10 个 SCLK，对应的是地址，数据为 00_0000_0001，表示写的是 001 寄存器。再接着的 32 个 SCLK， 对应的数据是 14,18,31,02 表示写入 01 寄存器的数值为 32'h14183102. 最后的 8 个 SCLK， 对应的 SDI 为 0， 是无用的数据。（SPI_CSH=1）

以 spi_rd_reg(10'h000,temp32b) 即读第 0 寄存器的结果为例，说明 SPI 读对应的波形：

前面 6 个 SCLK， 对应 SDI 为 6b0010_00，所以是 SPI 读命令。后面 10 个 SCLK，对应的是地址，数据为 00_0000_0000，表示读的是 SPI 000 寄存器。再接着的 8 个 SCLK, 对应 SDI 数据为 0，为 8bits dummy， 最后面的 32 个 SCLK， 对应的 SDI 数据是 0，而此时对应的 SDO 的输出为读出结果。（SPI_CSH =1）

测试激励信号是下降沿给 SDI 数据，芯片内部是上升沿抓数。芯片给出的 SDO 信号是 SCLK 上升沿给出，接收端下降沿去抓 SDO 结果。

7.3 典型特性 (Typical Characteristics)

CAE2400 典型特性

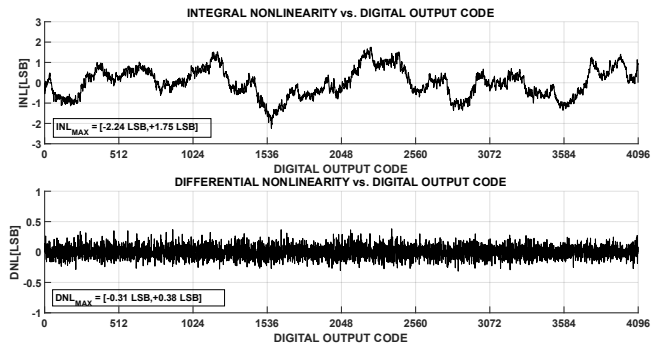


图 7-3. INL/DNL at Fin = 180MHz, 6GSPS (0.5Vpp FS)

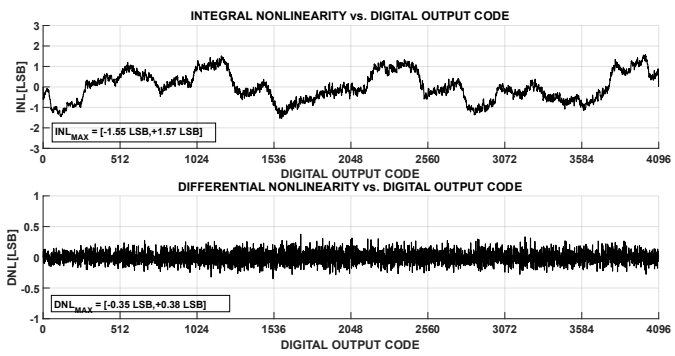


图 7-4. INL/DNL at Fin = 180MHz, 6GSPS (0.8Vpp FS)

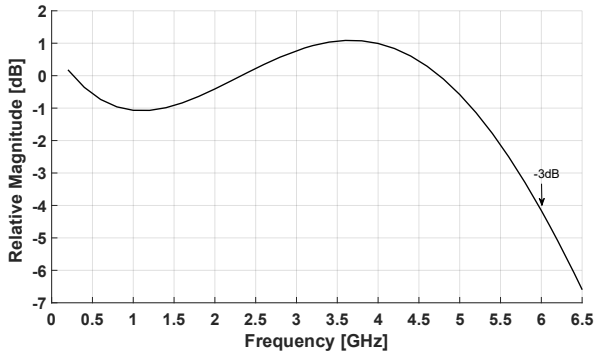


图 7-5. Relative Magnitude vs Input Frequency

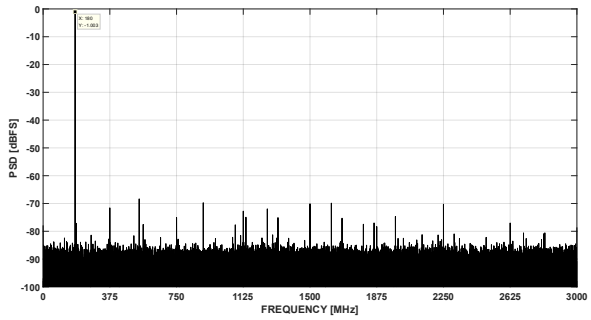


图 7-6. FFT at Fin = 180MHz, 6GSPS (0.5Vpp FS, -1 dBFS)

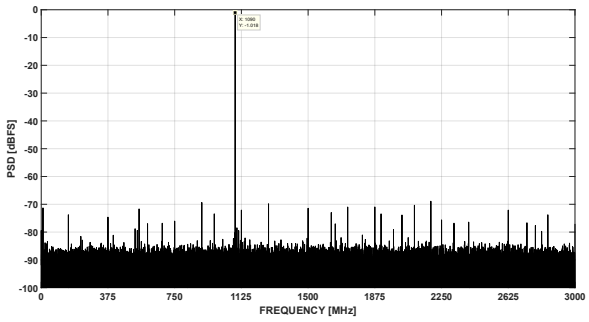


图 7-3. FFT at Fin = 1.09GHz, 6GSPS (0.5Vpp FS, -1 dBFS)

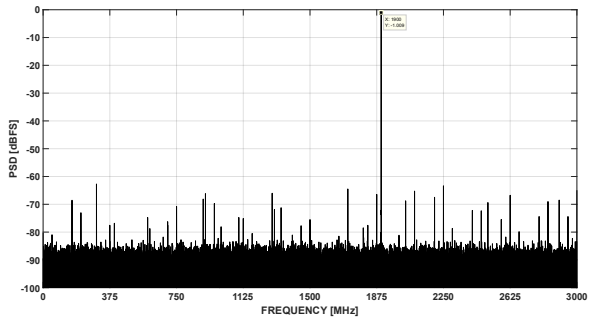


图 7-4. FFT at Fin = 1.9GHz, 6GSPS (0.5Vpp FS, -1 dBFS)

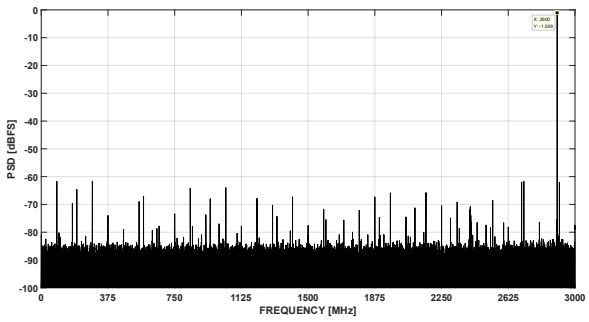


图 7-9. FFT at Fin = 2.9GHz, 6GSPS (0.5Vpp FS, -1 dBFS)

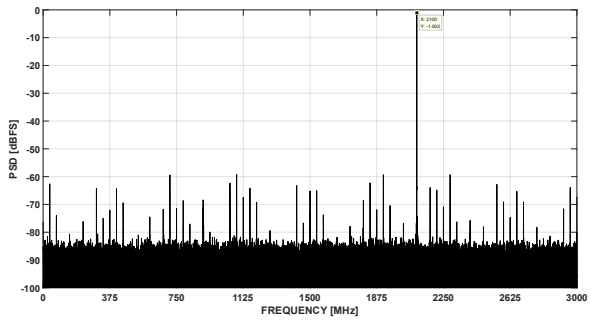


图 7-10. FFT at Fin = 3.9GHz, 6GSPS (0.5Vpp FS, -1 dBFS)

CAE2400 典型特性 (Continued)

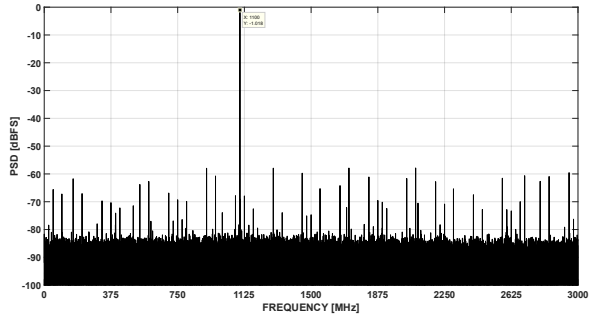


图 7-11. FFT at Fin = 4.9GHz, 6GSPS (0.5Vpp FS, -1 dBFS)

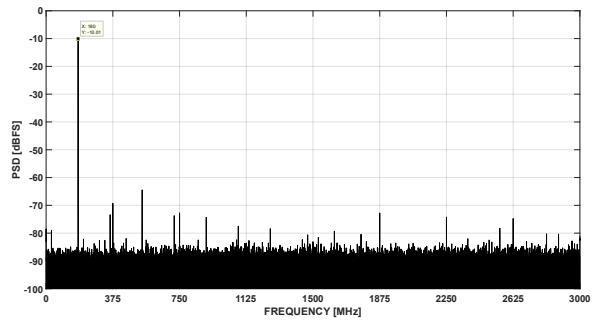


图 7-12. FFT at Fin = 180MHz, 6GSPS (0.5Vpp FS, -10 dBFS)

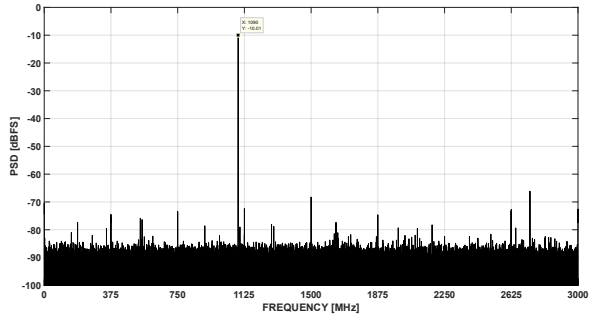


图 7-13. FFT at Fin = 1.09GHz, 6GSPS (0.5Vpp FS, -10 dBFS)

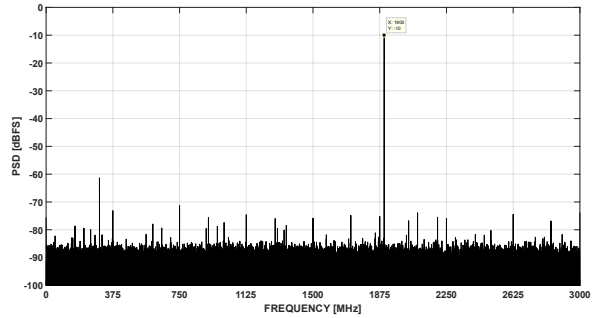


图 7-14. FFT at Fin = 1.9GHz, 6GSPS (0.5Vpp FS, -10 dBFS)

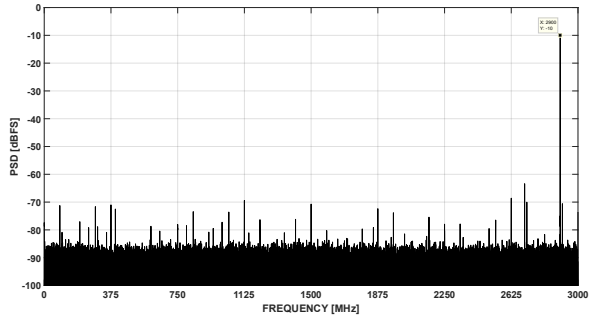


图 7-15. FFT at Fin = 2.9GHz, 6GSPS (0.5Vpp FS, -10 dBFS)

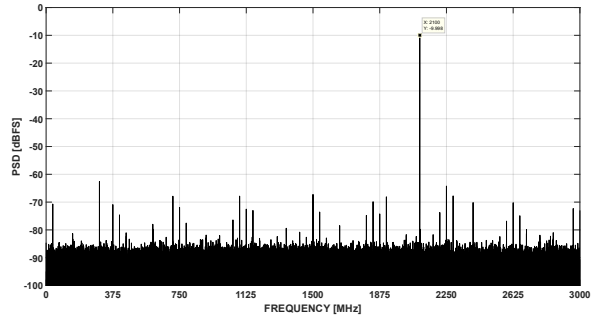


图 7-16. FFT at Fin = 3.9GHz, 6GSPS (0.5Vpp FS, -10 dBFS)

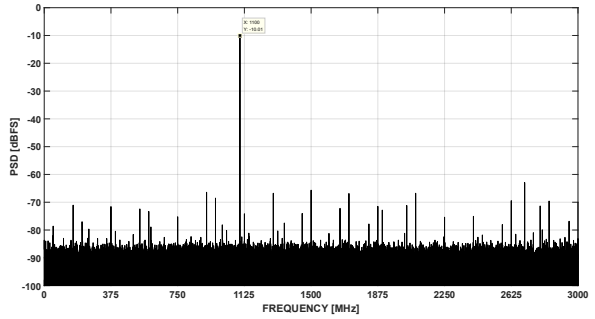


图 7-15. FFT at Fin = 4.9GHz, 6GSPS (0.5Vpp FS, -10 dBFS)

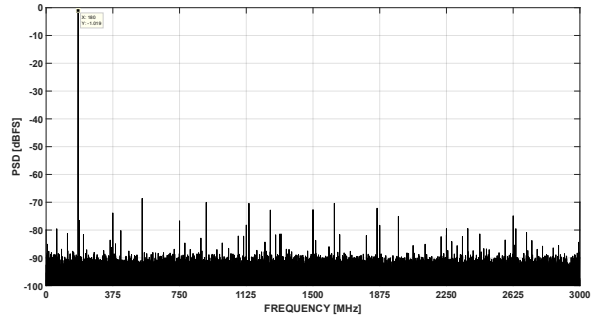


图 7-18. FFT at Fin = 180MHz, 6GSPS (0.8Vpp FS, -1 dBFS)

CAE2400 典型特性 (Continued)

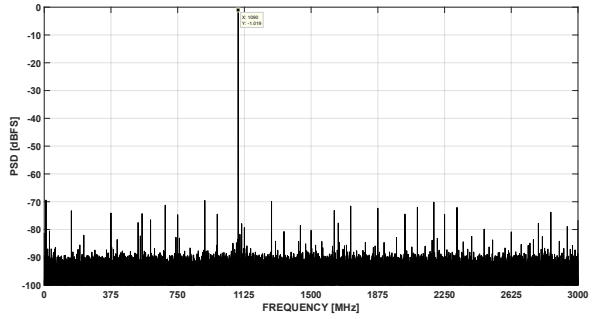


图 7-19. FFT at Fin = 1.09GHz, 6GSPS (0.8Vpp FS, -1 dBFS)

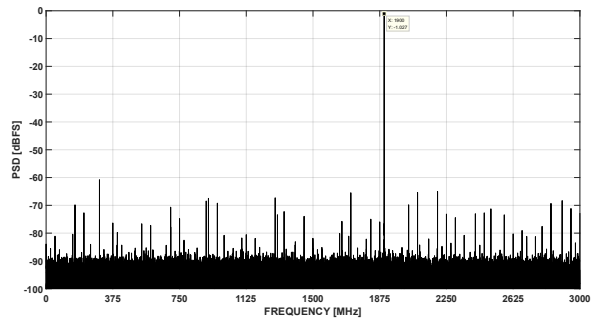


图 7-20. FFT at Fin = 1.9GHz, 6GSPS (0.8Vpp FS, -1 dBFS)

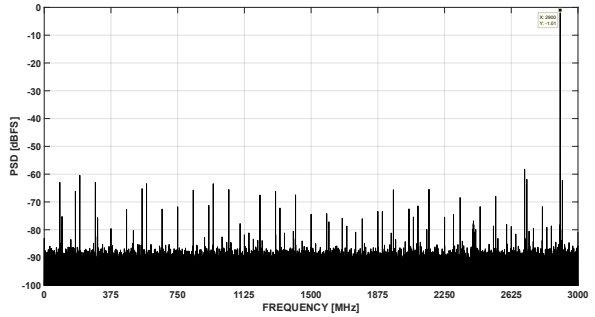


图 7-21. FFT at Fin = 2.9GHz, 6GSPS (0.8Vpp FS, -1 dBFS)

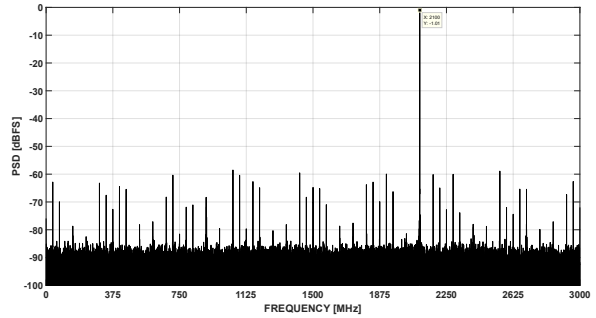


图 7-22. FFT at Fin = 3.9GHz, 6GSPS (0.8Vpp FS, -1 dBFS)

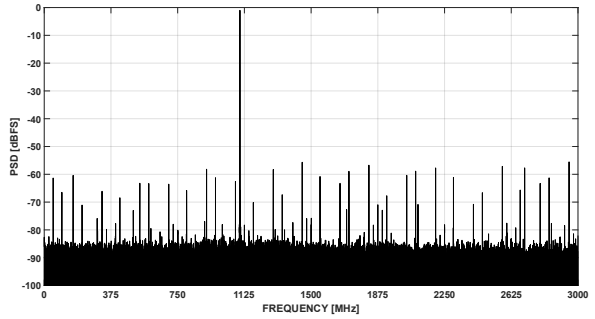


图 7-23. FFT at Fin = 4.9GHz, 6GSPS (0.8Vpp FS, -1 dBFS)

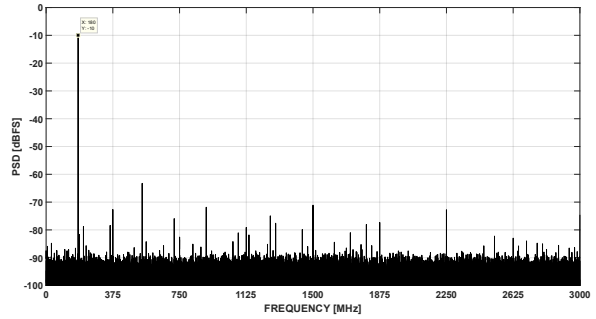


图 7-24. FFT at Fin = 180MHz, 6GSPS (0.8Vpp FS, -10 dBFS)

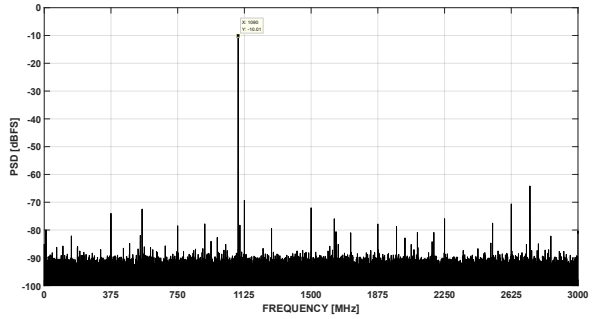


图 7-25. FFT at Fin = 1.09GHz, 6GSPS (0.8Vpp FS, -10 dBFS)

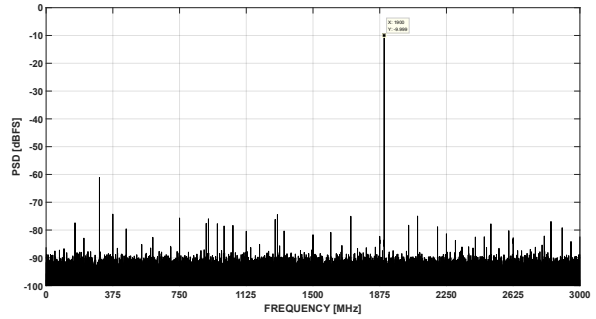


图 7-26. FFT at Fin = 1.9GHz, 6GSPS (0.8Vpp FS, -10 dBFS)

CAE2400 典型特性 (Continued)

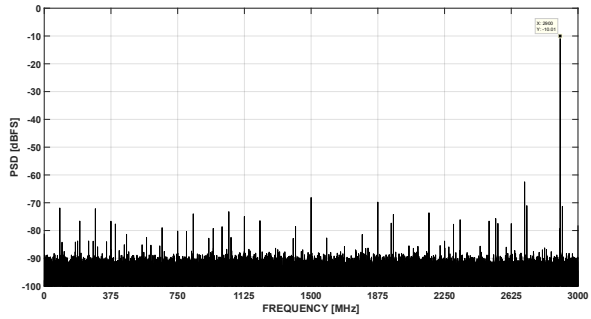


图 7-27. FFT at Fin = 2.9GHz, 6GSPS (0.8Vpp FS, -10 dBFS)

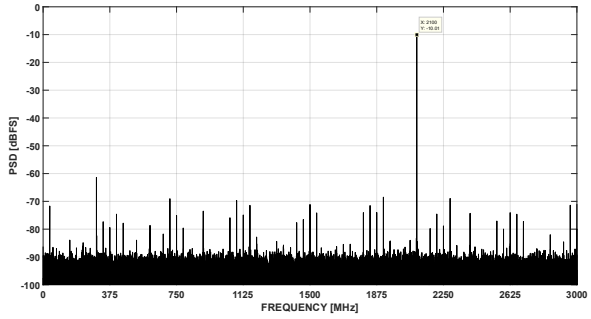


图 7-28. FFT at Fin = 3.9GHz, 6GSPS (0.8Vpp FS, -10 dBFS)

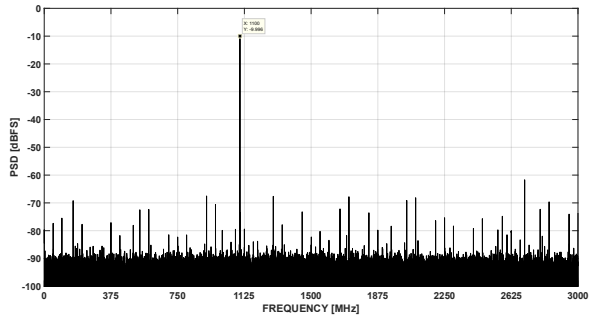


图 7-29. FFT at Fin = 4.9GHz, 6GSPS (0.8Vpp FS, -10 dBFS)

8 详细说明 (Detailed Description)

8.1 概述 (Overview)

CAE2400 是一款 12 位，高速射频采样模数转换器 (ADC)，单通道模式下的最大采样率 6GSPS，双通道下的最大采样率为 3GSPS。

单通道或者双通道工作模式可在线编程配置，可用于开发灵活的硬件，以满足高通道数或宽瞬时信号带宽应用的需求。

CAE2400 采用高速 JESD204B 输出接口，工作温度（结温）支持 -40 to 115°C，使用 FCBGA196 (12mm x 12mm) 封装。

8.2 功能框图 (Functional Block Diagram)

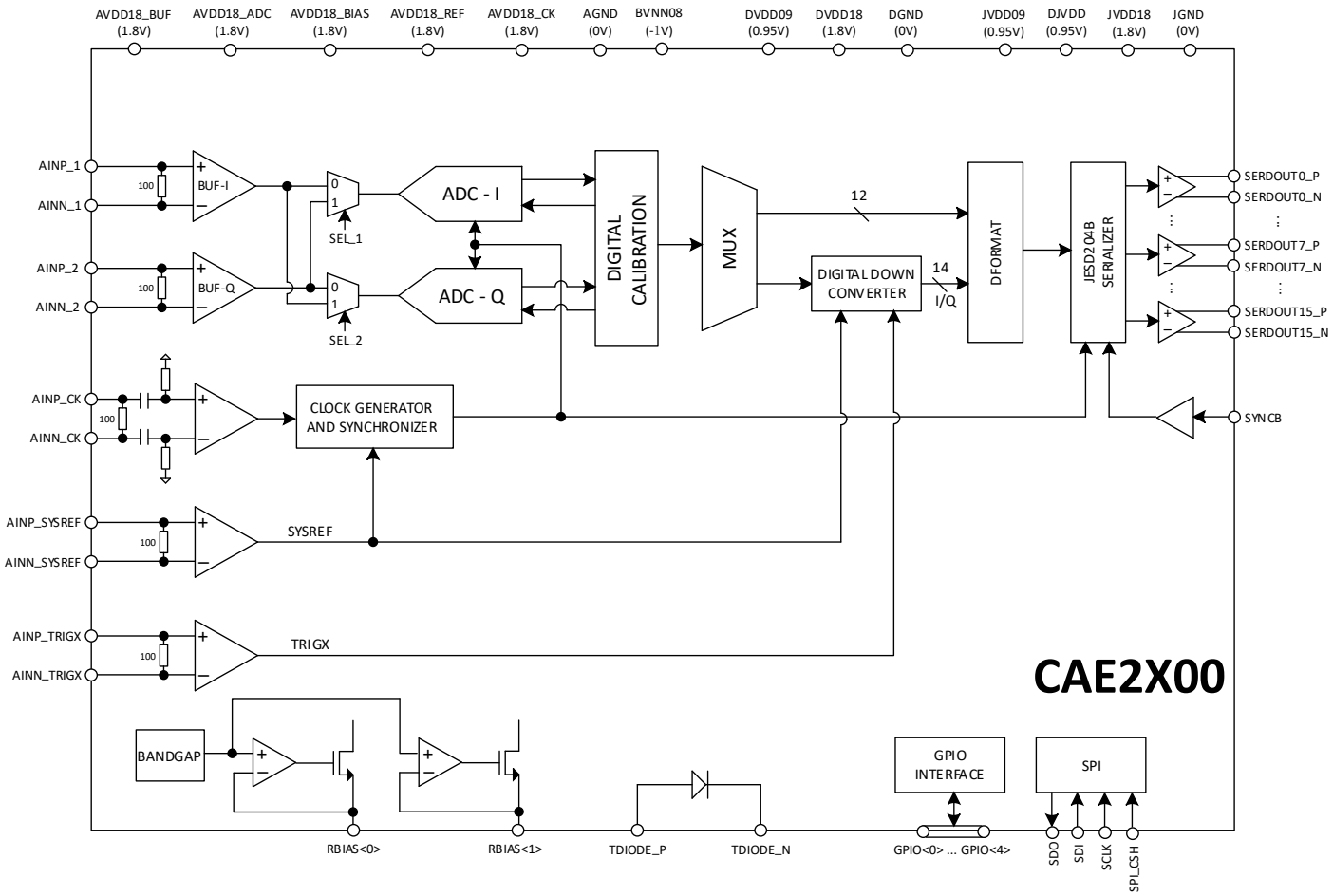


图 8-1. 功能框图

8.3 信号管脚连接说明

CAE2400 信号管脚按功能类型可分为以下 9 类:

表 8-1. CAE2400 信号管脚分类

类别序号	信号管脚类别	管脚数量	信号管脚名称
1	模拟信号输入管脚	4	AINP_1 / AINN_1 AINP_2 / AINN_2
2	主时钟输入管脚	2	AINP_CK / AINN_CK
3	SYSREF 同步信号输入管脚	2	AINP_SYSREF / AINN_SYSREF
4	TRIGX 信号输入管脚	2	AINP_TRIGX / AINN_TRIGX
5	模拟参考偏置电流管脚	2	RBIAS<0> 、RBIAS<1>
6	温度二极管管脚	2	TDIODE_P / TDIODE_N
7	数字 IO 输入管脚(1.8V 电平)	13	RESET_ANALOG 、RESET_LOGIC TSKEW_BG 、GPIO<0> GPIO<1> 、GPIO<2> GPIO<3> 、GPIO<4> SDI 、SCLK 、SPI_CSH POWERDOWN 、SYNCB
8	数字 IO 输出管脚(1.8V 电平)	3	FD<0> 、FD<1> 、SDO
9	JESD204B SerDes 高速输出管脚	32	SERDOUT0_P / SERDOUT0_N SERDOUT1_P / SERDOUT1_N SERDOUT2_P / SERDOUT2_N SERDOUT3_P / SERDOUT3_N SERDOUT4_P / SERDOUT4_N SERDOUT5_P / SERDOUT5_N SERDOUT6_P / SERDOUT6_N SERDOUT7_P / SERDOUT7_N SERDOUT8_P / SERDOUT8_N SERDOUT9_P / SERDOUT9_N SERDOUT10_P / SERDOUT10_N SERDOUT11_P / SERDOUT11_N SERDOUT12_P / SERDOUT12_N SERDOUT13_P / SERDOUT13_N SERDOUT14_P / SERDOUT14_N SERDOUT15_P / SERDOUT15_N

8.3.1 模拟信号输入管脚 AINP_1 / AINN_1 、AINP_2 / AINN_2

模拟信号输入管脚支持交流（AC）耦合以及直流（DC）耦合两种连接方式。

其中 **AINP_1 / AINN_1** 为模拟输入通道 1 的差分输入端口，**AINP_2 / AINN_2** 为模拟输入通道 2 的差分输入端口。

每个模拟输入通道内建有 100 欧姆差分端接电阻。

内部钳位二极管可防止输入信号功率过高导致模拟输入通道上器件被烧毁。

PCB 上连接至模拟信号输入管脚的走线需严格按照单端 50 欧姆 / 差分 100 欧姆做好阻抗控制，不合理的走线阻抗会导致模拟输入信号产生严重的反射。同时，模拟输入信号的 PCB 走线应尽量避免经过通孔，并做好隔离，防止其他信号线或者噪声较大的电源干扰。

为了减少 PCB 走线对模拟输入信号的损耗，PCB 板材尽可能选用高频/高速板材，例如 Rogers 的 RO4350B 或者松下的 M6 等。

交流（AC）耦合连接说明

如**图 8-2** 所示，当交流（AC）耦合连接时，模拟信号输入管脚需外部提供 0.45V 差分输入共模电压（VCMI）。该 VCMI 电压可以通过外部电阻分压产生，并通过 2K 欧电阻连接至模拟信号输入管脚。

需要注意，两个模拟输入通道的 VCMI 必须各自独立。共用 VCMI 可能导致两个模拟通道之间相互干扰。

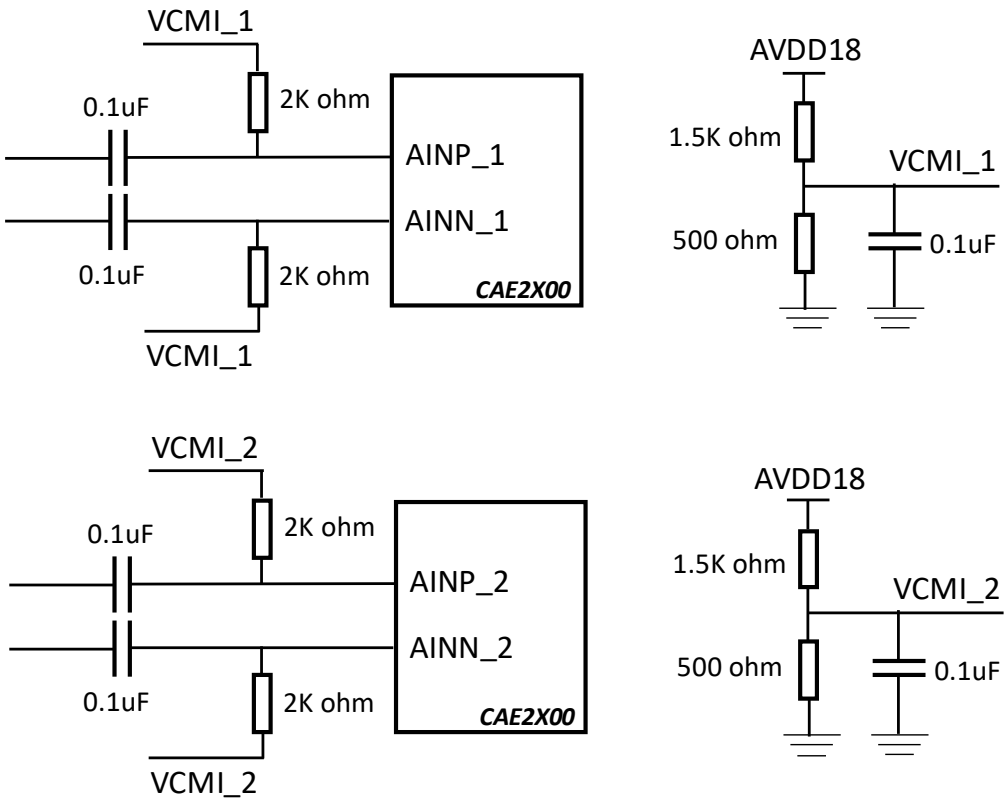


图 8-2. 模拟信号输入管脚交流（AC）耦合连接示意图

直流（DC）耦合连接说明

如**图 8-3** 所示，当直流（DC）耦合连接时，模拟信号输入管脚可以直连模拟前端的差分输出（例如差分运放输出），但该模拟前端的差分输出共模电压需为 0.45V。

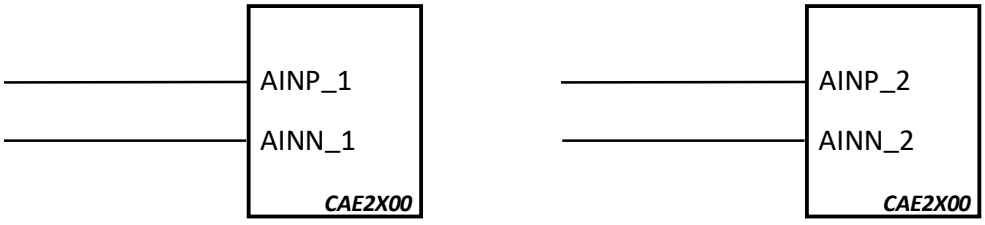


图 8-3. 模拟信号输入管脚直流（DC）耦合连接示意图

8.3.2 主时钟输入管脚 AINP_CK / AINN_CK

主时钟输入管脚 **AINP_CK / AINN_CK** 仅支持交流（AC）耦合连接方式。

如**图 8-4** 所示，高频输入时钟通过 0.1uF 隔直电容，交流耦合至 **AINP_CK / AINN_CK**。

为了最大化输入时钟的摆幅，主时钟输入管脚需外部提供差分共模电压（VCM_CLK），该 VCM_CLK 可以通过外部电阻分压产生，分压电源（VDD_CLK）需使用时钟电源或者单独的电源，避免使用 ADC 的 1.8V 模拟电源，以便减小时钟对模拟输入通路的干扰。

时钟通路内部有 100 欧姆端接电阻。

PCB 上连接至主时钟输入管脚的走线需严格按照单端 50 欧姆 / 差分 100 欧姆做好阻抗控制，不合理的走线阻抗会导致主时钟输入信号产生严重的反射。

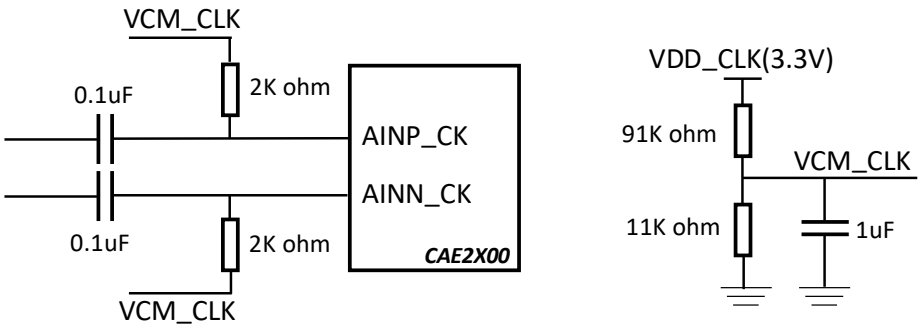


图 8-4. 主时钟输入管脚交流（AC）耦合连接示意图

8.3.3 SYSREF 同步信号输入管脚 AINP_SYSREF / AINN_SYSREF

SYSREF 同步信号输入管脚支持交流（AC）耦合以及直流（DC）耦合两种连接方式。

该差分输入管脚内部有 100 欧姆端接电阻，并且内部有共模电压产生电路，无需外部提供共模电压。

图 8-5 为该差分输入管脚的连接示意图。

PCB 上连接至 SYSREF 同步信号输入管脚的走线需严格按照单端 50 欧姆 / 差分 100 欧姆做好阻抗控制，不合理的走线阻抗会导致 SYSREF 同步信号输入信号产生严重的反射。

该 SYSREF 同步信号需要由支持产生 SYSREF 信号的时钟芯片产生。

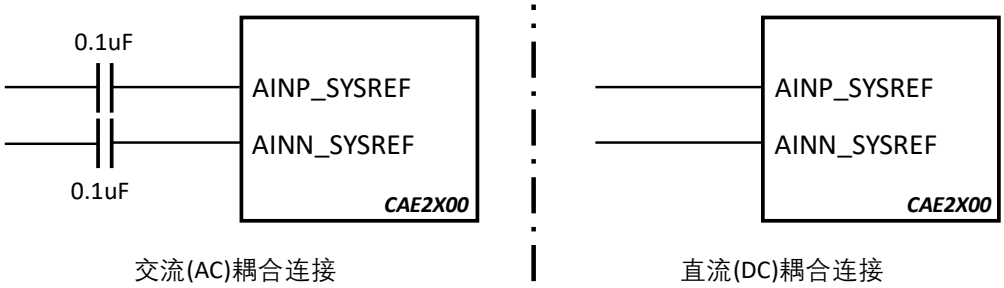


图 8-5. SYSREF 同步信号输入管脚交流（AC）耦合 / 直流（DC）耦合连接示意图

8.3.4 TRIGX 信号输入管脚 AINP_TRIGX / AINN_TRIGX

TRIGX 信号输入管脚支持交流（AC）耦合以及直流（DC）耦合两种连接方式。

该差分输入管脚内部有 100 欧姆端接电阻，并且内部有共模电压产生电路，无需外部提供共模电压。

图 8-6 为该差分输入管脚的连接示意图。

PCB 上连接至 TRIGX 信号输入管脚的走线需严格按照单端 50 欧姆 / 差分 100 欧姆做好阻抗控制，不合理的走线阻抗会导致 TRIGX 信号输入信号产生严重的反射。

该 TRIGX 信号可以通过 FPGA 的差分输出 IO 产生。

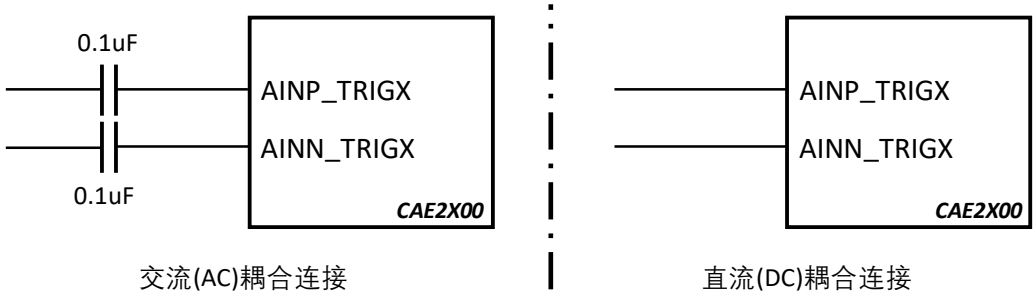


图 8-6. TRIGX 信号输入管脚交流（AC）耦合 / 直流（DC）耦合连接示意图

8.3.5 模拟参考偏置电流管脚 RBIAS<0> 、RBIAS<1>

RBIAS<0> 、**RBIAS<1>**用于产生模拟电路内部精准参考偏置电流。
如**图 8-7** 所示，每个管脚各通过一个 12K 欧姆电阻接地。
该 12K 电阻的精度需要小于或等于 1%（0.1%精度更佳），同时电阻温度系数需要小于或等于 25ppm。
12K 电阻推荐使用 0402 或者 0201 封装。
PCB 上该 12K 电阻需尽量靠近芯片管脚放置，以减小走线长度。同时做好隔离，避免噪声信号或者电源干扰。

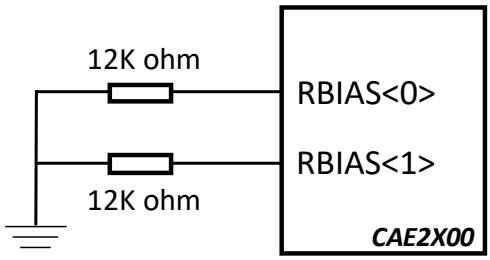


图 8-7. 模拟参考偏置电流管脚 RBIAS<0> 、RBIAS<1>连接示意图

8.3.6 温度二极管管脚 TDIODE_P / TDIODE_N

TDIODE_P / TDIODE_N 为 CAE2400 芯片内部温度二极管管脚。
如**图 8-8** 所示，该管脚可连接至外部测温芯片，以实时监控 CAE2400 内部结温，防止芯片内部过热导致性能下降或者老化。图中串联电阻 **Rs** 以及差分电容 **Cdiff** 的数值需要根据实际所选的测温芯片的要求决定。

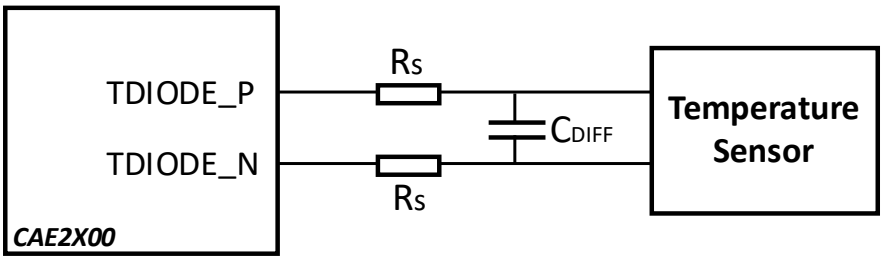


图 8-8. 温度二极管管脚 TDIODE_P / TDIODE_N 连接示意图

8.3.7 数字 IO 输入管脚（1.8V 电平）RESET_ANALOG、RESET_LOGIC、TSKEW_BG、GPIO<0>、GPIO<1>、GPIO<2>、GPIO<3>、GPIO<4>、SDI、SCLK、SPI_CSH、POWERDOWN、SYNCB

CAE2400 一共有 13 个数字 IO 输入管脚。每个管脚的具体功能请参考**表 6-1**。
目前 5 个 GPIO 引脚仅支持输入功能，不支持输出。
如**图 8-9** 所示，13 个数字 IO 输入管脚通过可选的 0 欧姆电阻连接至 FPGA 的 1.8V 电平 IO 管脚。如果 FPGA 的 IO 管脚不是 1.8V 电平，则需通过外部电平转换芯片转换成 1.8V 电平的 IO，再连接至 CAE2400 的数字 IO 管脚。
RESET_ANALOG 以及 RESET_LOGIC 管脚，可以在 PCB 上增加复位按钮电路（下图红色虚线框），通过板载按钮开关实现硬件快速复位。
不使用的数字 IO 输入管脚需要接地或者接 1.8V 高电平处理，避免悬空。

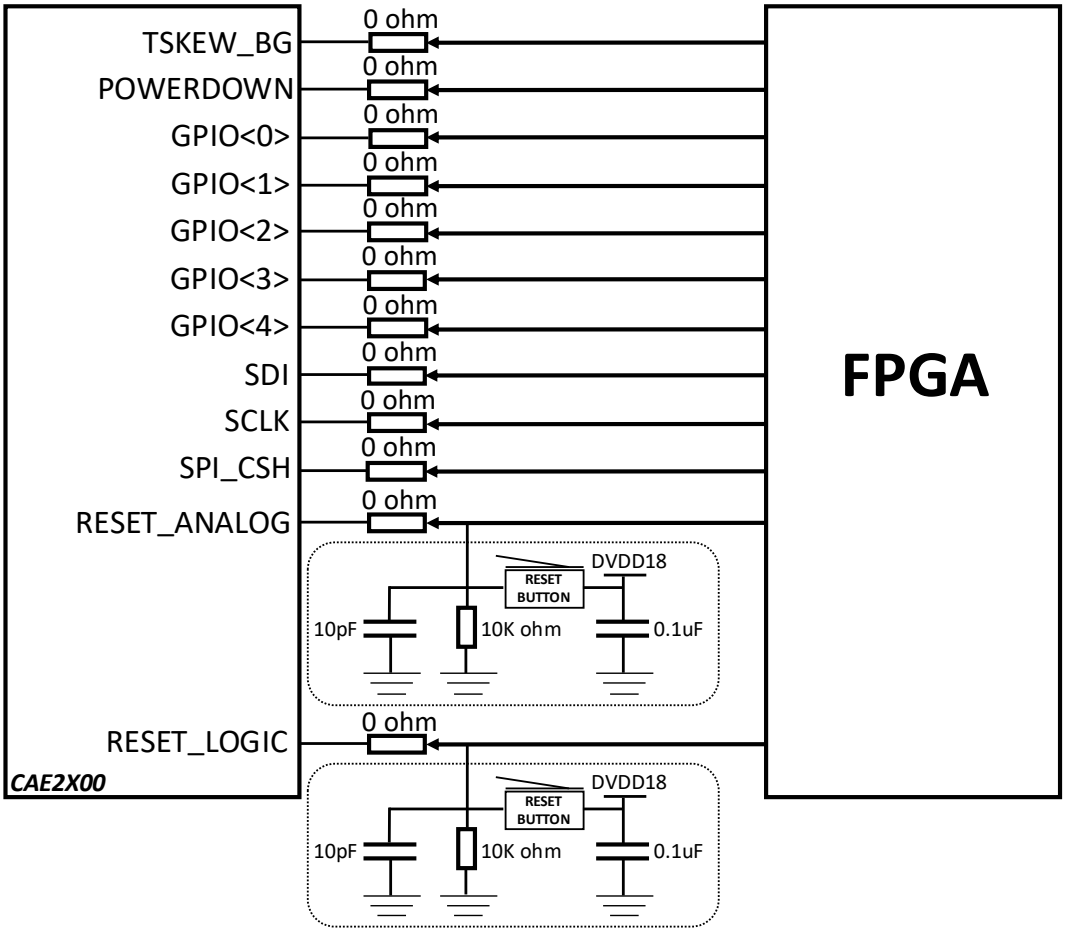


图 8-9. 数字 IO 输入管脚（1.8V 电平）连接示意图

8.3.8 数字 IO 输出管脚（1.8V 电平）FD<0>、FD<1>、SDO

CAE2400 一共有 3 个数字 IO 输出管脚。每个管脚的具体功能请参考**表 6-1**。
如**图 8-10** 所示，3 个数字 IO 输出管脚通过可选的 0 欧姆电阻连接至 FPGA 的 1.8V 电平 IO 管脚。
如果 FPGA 的 IO 管脚不是 1.8V 电平，则需通过外部电平转换芯片转换成 1.8V 电平的 IO。
不使用的数字 IO 输出管脚可以悬空。但不能直接接地或者接高电位。

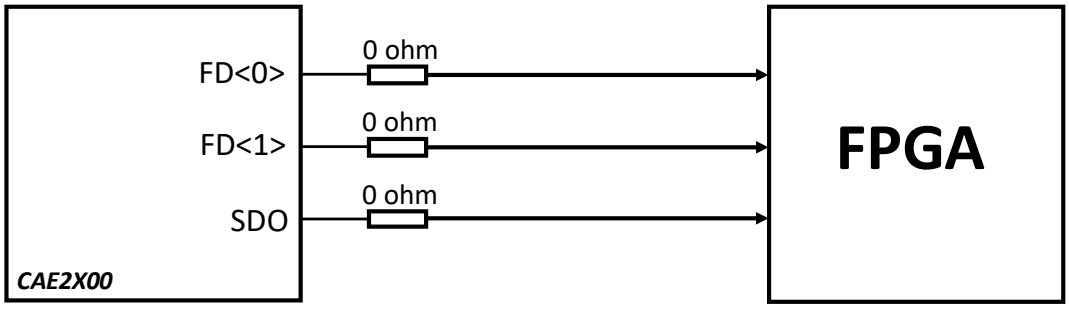


图 8-10. 数字 IO 输出管脚（1.8V 电平）连接示意图

8.3.9 JESD204B SerDes 高速输出管脚

SERDOUT0_P / SERDOUT0_N、SERDOUT1_P / SERDOUT1_N、SERDOUT2_P / SERDOUT2_N
SERDOUT3_P / SERDOUT3_N、SERDOUT4_P / SERDOUT4_N、SERDOUT5_P / SERDOUT5_N
SERDOUT6_P / SERDOUT6_N、SERDOUT7_P / SERDOUT7_N、SERDOUT8_P / SERDOUT8_N
SERDOUT9_P / SERDOUT9_N、SERDOUT10_P / SERDOUT10_N、SERDOUT11_P / SERDOUT11_N

SERDOUT12_P / SERDOUT12_N 、SERDOUT13_P / SERDOUT13_N 、SERDOUT14_P / SERDOUT14_N SERDOUT15_P / SERDOUT15_N

CAE2400 一共有 16 lane JESD204B SerDes 高速输出管脚。

如**图 8-11** 所示，每个管脚通过 0.1uF 隔直电容交流耦合连接至 FPGA 的 RX 高速收发器。

PCB 上 16 lane SerDes 走线需严格按照单端 50 欧姆 / 差分 100 欧姆做好阻抗控制。并且 16 lane 之间需做等长处理。

SerDes 的 lane 与 lane 之间需保证有不低于-33dB 的 隔离度。

为减少 SerDes 信号的走线损耗，PCB 板材需要选用高频/高速板材，例如 Rogers 的 RO4350B 或者松下的 M6 等。

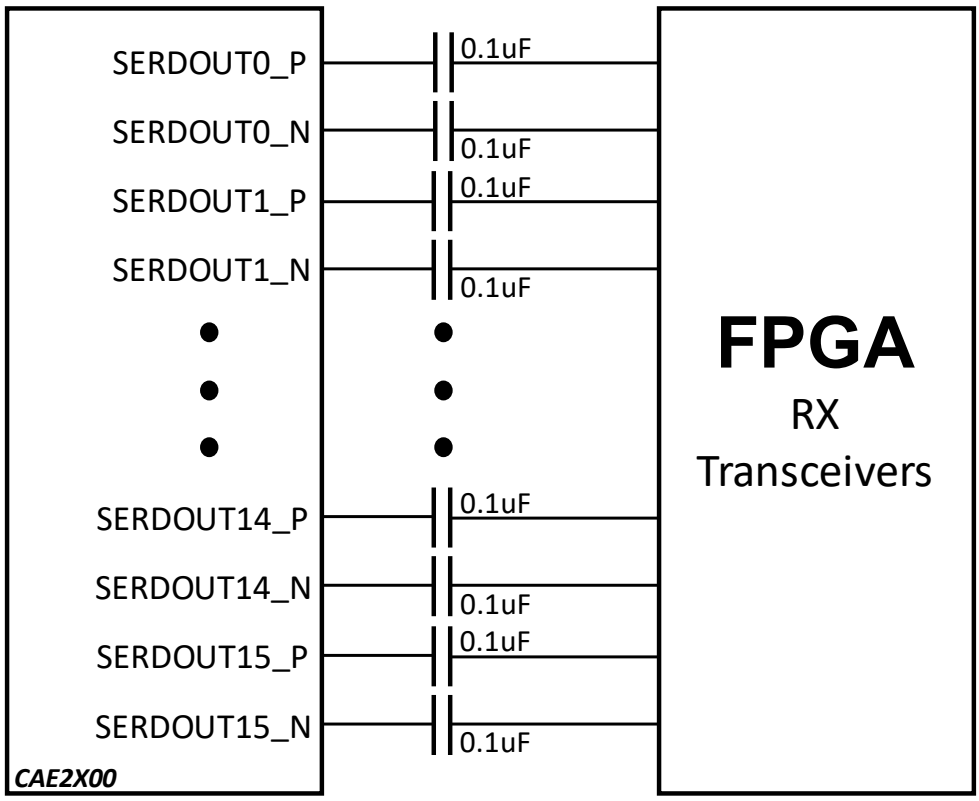


图 8-11. JESD204B SerDes 高速输出管脚连接示意图

8.4 电源连接说明

CAE2400 有 12 组 **1.8V** 电源，3 组 **0.95V** 电源，2 组**-1V** 负电源。

图 8-12 是 **CAE2400** 各电源完全分离连接的方案示意图。

图中由 12V 电源适配器连接到 3 个 DCDC，再通过 4 个 LDO 产生 11 路电源给到 **CAE2400**。

其中 **CAE2400** 模拟电路电源按照模块划分为 5 组（**AVDD18_BUF**、**AVDD18_ADC**、**AVDD18_REF**、**AVDD18_BIAS**、**AVDD18_CK**）。5 组模拟电源由单独的 LDO 产生，并通过磁珠（Ferrite Bead）或者馈通电容滤波器（Feed through filter）分离 5 组电源。

DVDD18 与 **JVDD18** 可以共用一个 LDO，但是需要通过磁珠（Ferrite Bead）或者馈通电容滤波器（Feed through filter）分离这两路电源。

DVDD09、**DJVDD**、**JVDD09** 可以共用一个 LDO，但是需要通过磁珠（Ferrite Bead）或者馈通电容滤波器（Feed through filter）分离这三路电源。

BVNN08<0>与 **BVNN08<1>**需要在 PCB 上连接到一起，并由同一路负电源供电。分开供电可能导致两路负电源出现电位差，从而影响性能。

PCB 上 CAE2400 芯片底部各电源的电流应不低于图中的推荐值（该数值非实际电源电流值），并尽可能留有余量，确保电源走线寄生电阻小。较大的电源平面也有助于散热。

上电顺序需要保证 **1.8V** 电源先于 **0.95V** 电源上电。如果 **0.95V** 电源先上电，可能导致数字 IO 管脚出现漏电。尽量避免出现只有 **0.95V** 电源上电但是 **1.8V** 电源没有上电的情况，数字 IO 持续性的漏电可能导致芯片出现不可逆的损坏。

AGND、**DGND**、**JGND** 三个地需要在 PCB 上短接在一起。

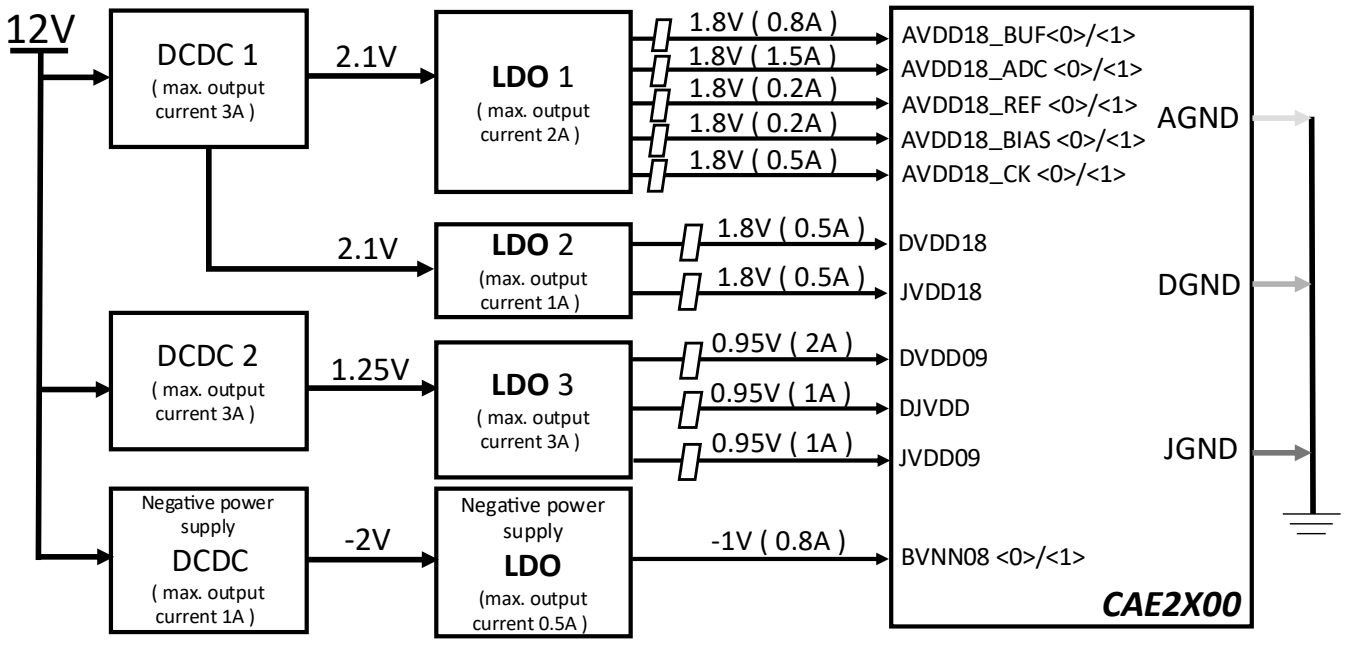


图 8-12. CAE2400 推荐电源连接示意图

（注意：图中 DCDC 到 LDO 的输出电压值仅为参考，具体电压值需根据实际使用的 DCDC 器件以及 LDO 器件决定**）**

图 8-13 是 **CAE2400** 电源部分合并连接的方案示意图。

图中 LDO1 通过磁珠分出两路 1.8V 电源，其中 **AVDD18_BUF**、**AVDD18_ADC**、**AVDD18_REF**、**AVDD18_BIAS** 共用一路 1.8V 电源，**AVDD18_CK** 则单独用一路 1.8V 电源。

LDO3 通过磁珠分出两路 0.95V 电源。其中 **DJVDD** 与 **JVDD09** 共用 1 路 0.95V 电源。

PCB 上 CAE2400 芯片底部各电源的电流应不低于图中的推荐值（该数值非实际电源电流值），并尽可能留有余量，确保电源走线寄生电阻小。较大的电源平面也有助于散热。

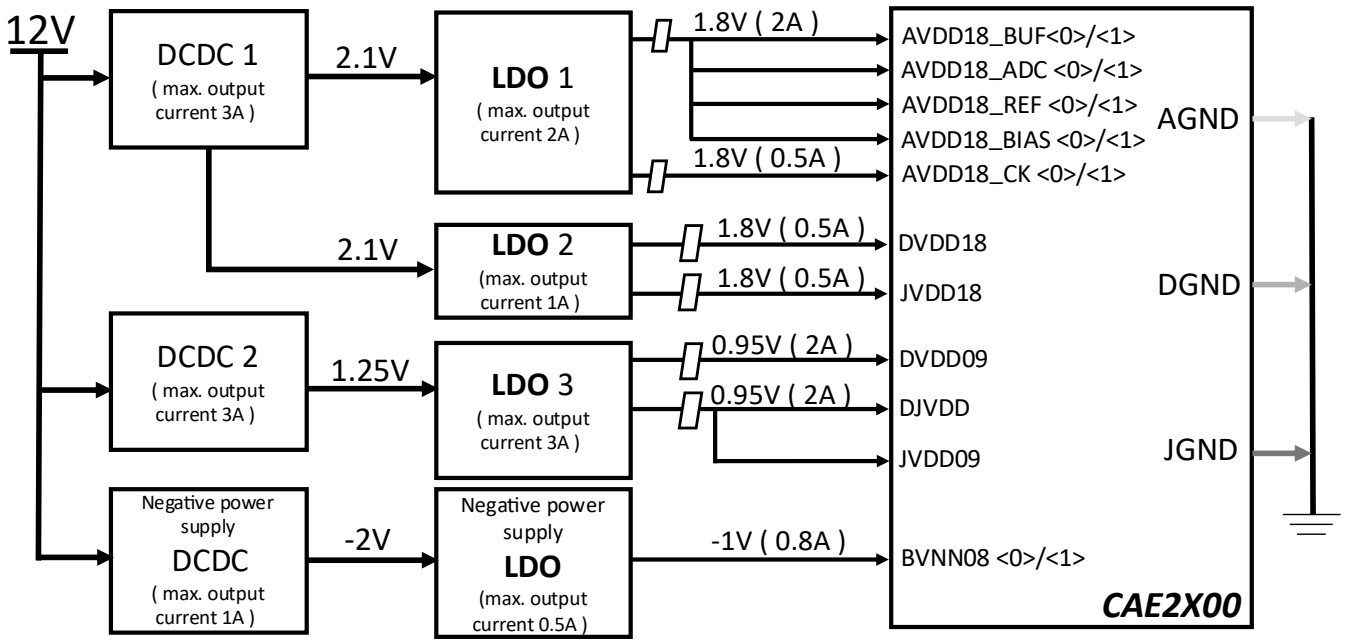


图 8-13. CAE2400 推荐合并电源连接示意图

8.5 电源滤波电容放置说明

CAE2400 各组电源在 PCB 上需要就近放置滤波电容以减小电源波动对 ADC 性能的影响。

图 8-14 是 **CAE2400** 电源管脚滤波电容就近放置的参考示意图。图中默认 PCB 采用树脂塞孔工艺，且滤波电容封装尺寸为 0201，此时滤波电容可以放置在 PCB 背面 **CAE2400** 的电源管脚与 GND 管脚位置。

需要注意的是，图中 **NC** 管脚与 **DJVDD** 管脚位置的电容，仅表示当 **NC** 管脚为悬空状态且焊盘上没有通孔，PCB 背面 **NC** 管脚下方实际是 GND 时，该位置可以放置一个 0201 封装的滤波电容。将 **NC** 管脚接地或者用电容连接 **NC** 管脚与 **DJVDD** 电源管脚都可能导致 ADC 芯片无法工作。

图中 **AVDD18** 的电容位置为 PCB 上建议预留的电容焊盘位。实际表贴的电容数量可以根据具体的电源以及布线情况调整。如果电容位置不是全部表贴上电容的话，则表贴的电容需要尽可能交错均匀放置，尽量避免只在某一边或者某几个电源管脚上放置电容。

DVDD18 以及 **JVDD18** 电源建议在靠近 ADC 芯片附近增加一到两个电容位。

滤波电容建议使用一个 1uF 配多个 0.1uF 的组合。以便减少电源的低频高频噪声。

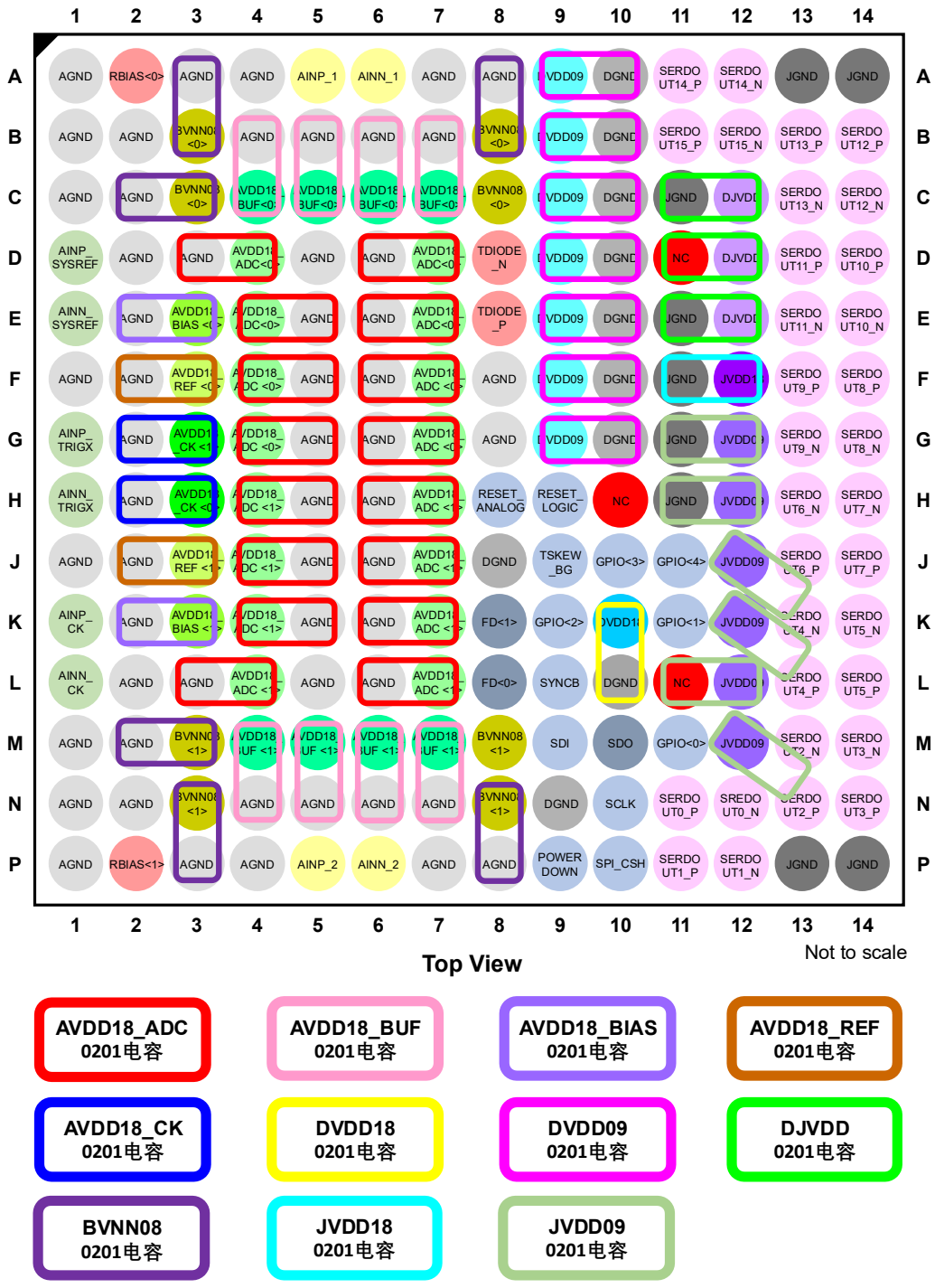


图 8-14. CAE2400 推荐各电源滤波电容放置参考示意图

（注意：图中 NC 管脚为悬空状态，无任何连接且无任何过孔在管脚位。）

9 寄存器说明 (Memory Map)

9.1 SPI 控制寄存器说明

表 9-1. SPI 控制寄存器列表

No.	Register Name	Register Address	Default Value
1	Timing Skew 控制寄存器	0x005	32'h0042_9648
2	Output Mode 控制寄存器	0x006	32'h4000_7958
3	Aperture Delay 寄存器	0x089	
4	FD dwell 寄存器	0x15F	32'h0000_0000
5	FS Range A 控制寄存器	0xE2	32'h5A40_0001
6	FS Range B 控制寄存器	0xE3	32'h5A40_0001
7	Fast Threshold Detection 寄存器	0x15E	32'h0000_0000
8	Analog input channel 寄存器	0x002	32'h8003_8FFF
9	DDC NCO 控制寄存器	0x07	32'h0301_0000
10	DDC PHASE 控制寄存器		
11	DDC FTW 控制寄存器		
12	DDC 控制寄存器	0x001	32'h8000_4000
13	DDC PST 控制寄存器	0x1C	32'h0010_0000
14	JESD204B MAC 寄存器	0x200-0x27F	
15	JESD204B PMA PHY 寄存器	0x280-0x2FF	

Timing Skew 控制寄存器（地址 9h05 32' h0042_9648）

Bits	Name	Default	Descriptions
31	bg_always	1'b0	Background timing skew always do 1 : enable 0 : disable
30	bg_fpga	1'b0	FPGA background timing skew enable 1 : enable 0 : disable
29	tskew_hd_en	1'b0	Tskew_bg_pin is enable to control background timing skew 1 : enable 0 : disable
28:27	Uf_range	2'h00	Ultra_fine range : 00 : 1 01 : 2 10 : 3 11 : 4
26:24	bgpd_mode	3'h000	Background timing skew power down timing set 000 : 50ms 001 : 100ms 010 : 200ms 011 : 300ms 100 : 700ms 101 : 1500ms 110 : 3100ms 111 : 6300ms
23	Ufwin_en	1'b0	Ultra_fine_detect window function(check ultra fine cap margin of stable) enable 1 : enable 0 : disable
22:20	tsrx_th	3'b100	Timing skew matrix result/N 000 : 1 001 : div2 010 : div4 011 : div8 100 : div16
19	tsfir_en	1'b0	1 : Timing skew input FIR enable 0 : disable (default)
18	Dual_mode	1'b0	1 : dual channel mode 0 : single channel mode(default)
17	fg_mode_spi	1'b1	Force finecap msb result=1 1 : enable 0 : disable

Timing Skew 控制寄存器（地址 9h05 32’ h0042_9648）(续)

Bits	Name	Default	Descriptions
16	sel_otp_data	1’b0	1 : Timing skew mode1/2 start from efuse value 0 : Timing skew mode1/2 start from current value
15:14	bg_thres	2’b10	Background timing skew result overflow threshold Lower threshold upper threshold 00 : 0 63 01 : 4 59 10 : 8 55 01 : 16 47
13:12	bg_mode	2’b01	background timing skew mode 00 : Used in factory test mode or Reset all 7b coarse, 6b fine and 6b ultra-fine codes mode 01 : Used in user mode (most often case): Keep the current 6b coarse and 6b fine codes, while loop [+1,0, -1] LSB on 6b ultrafine. This cases is looping programmable [8,16,32,64,128,256,512,1024] times, if it is still out of range or divergence, it goes to “10” mode 10 : Keep the current 6b coarse and 6b fine codes, reset all 6b ultra-fine code, first loop [+1,0, -1] LSB on 6b fine delay code and then loop [+1,0,-1] LSB on 6b ultra-fine delay code. If 6b fine after looping, it is out of range or divergence. It goes to “11” mode. Otherwise, if 6b fine is within pre-set range, only ultra-fine 6b codes are out of range. It goes to “01” mode. If both 6b fine codes and 6b ultra-fine codes are within pre-set range, it terminates the calibration. 11 : Reset all 6b fine and 6b ultra-fine codes mode, looping 7b coarse code. If 7b coarse codes are within pre-set range, it goes to loop 6b fine and then 6b ultra-fine. If 7b coarse codes are out of range, it goes to “00” mode.
11:8	tskew_mode	4’b0110	Timing skew discard/average samples setting 0000 : discard/average number 2^17 0001 : discard/average number 2^18 0010 : discard/average number 2^19 0011 : discard/average number 2^20 0100 : discard/average number 2^21 0101 : discard/average number 2^22 0110 : discard/average number 2^23 0111 : discard/average number 2^24 1000 : discard/average number 2^25 1001 : discard/average number 2^26 1010 : discard/average number 2^27 1011 : discard/average number 2^28 1100 : discard/average number 2^29 1101 : discard/average number 2^30 1110 : discard/average number 2^31 1111 : discard/average number 2^32
7	inv_ts_mode	1’b0	Timing skew sign result inverse 1 : enable 0 : disable
6:4	bg_ts_mode	3’b100	Background timing skew loop number 000 : 32loop 001 : 64loop 101 : 128loop 110 : 256loop 111 : 512loop
3:2	bg_repeat	2’b10	Decision loop number for majority result: Identical Trials Success Threshold 00 : 1 1 01 : 4 3 10 : 8 6 11 : 16 12
1	tskew_bg	1’b0	Background timing skew enable 1 : enable 0 : disable
0	RVD		

Output Mode 控制寄存器（地址 9h06 32’ h4000_7958）

Bits	Name	Default	Descriptions
31:8	RVD		
7	p2SnOf	1’b1	1 : output 2's code 0 : output offset code
6:0	RVD		

Aperture Delay 寄存器（地址 9h89）

Bits	Name	Default	Descriptions
31:23	aper_delay[8:0]	9'd0	Noiseless aperture delay (tAD) adjustment，average 5ps/step
22:0	RVD		

FD dwell 寄存器 （地址 9h15F 32'h0000_0000）

Bits	Name	Default	Descriptions
31:16	Fd_dwell_4B	16'h0	Sar4B dwell time counter target. The fast detect goes low if the analog input is below the fast detect lower threshold value for greater than this 16bits programmable data clock (fs/16 or dual mode fs/8) counter.
15:0	Fd_dwell	16'h0	Sar12b dwell time counter target. The fast detect goes low if the analog input is below the fast detect lower threshold value for greater than this 16bits programmable data clock (fs/16 or dual mode fs/8) counter.

FS Range A 控制寄存器（地址 9hE2 32'h5A40_0001）

Bits	Name	Default	Descriptions
31:22	Fs_range_A	10'h169	FS reference range setting for ADC_A
21:0	RVD		

FS Range B 控制寄存器（地址 9hE3 32'h5A40_0001）

Bits	Name	Default	Descriptions
31:22	Fs_range_B	10'h169	FS reference range setting for ADC_B
21:0	RVD		

Fast Threshold Detection 寄存器（地址 9h15E 32'h0000_0000）

Bits	Name	Default	Descriptions
31	RVD		
30:28	Fd4b_up	3'h0	Sar4B upper threshold. 4-bit value for the fast detect upper threshold. The fast detect goes high if the analog input(offset code high 4B) is above or equal with the upper threshold value for one data clock (fs/16 or dual mode fs/8） cycle. Fd4b_up sar4B offset code 000 1111 001 1110 010 1101 011 1100 100 1011 101 1010 110 1001 111 1000
26:16	Fd_up	11'h0	12B upper threshold. 11-bit value for the fast detect upper threshold. The fast detect goes high if the analog input(2s complement code abs value) is above the upper threshold value for one data clock (fs/16 or dual mode fs/8） cycle.
15:13	Fd4b_lo	3'h0	Sar4B lower threshold unsigned number. 4-bit value for the fast detect lower threshold. The fast detect goes low if the analog input(offset code high 4B) is below the lower threshold value for FD_dwell_4B time.
12	P4Bn12	1'b0	1 : sar4B mode 0 : 12b output data mode
11	fden	1'b0	Fast threshold detection enable 1 : enable 0 : disable
10:0	Fd_low	11'h0	Sar12B mode lower threshold unsigned number. 11-bit value for the fast detect lower threshold. The fast detect goes low if the analog input(2s complement code abs value) is below the lower threshold value for FD_dwell time.

Analog input channel 寄存器（地址 9h02 32'h8003_8FFF）

Bits	Name	Default	Descriptions
31:21	RVD		
20	SEL_BUF_CH	1'b0	analog buffer input setting for single channel mode 1 : Q_channel (AINP_2 / AINN_2) 0 : I_channel (AINP_1 / AINN_1)
19:0	RVD		

DDC NCO 控制寄存器 （地址 9h07 32'h0301_0000）

Bits	Name	Default	Descriptions
31:27	RVD		
26:24	sync_en, sync_next, trig_rst_en	3'b011	Register setting description SYSREF_x edge used to synchronize the PAWs 100 : all subsequent edges for SYSREF_x signal reset all the PAWs in the chip 110 : the next valid edge of SYSREF_x signal reset all the PAWs in the chip 001 : all edges of SYSREF_x signal after TRIGGER signal reset all the PAWs in the chip 011 : the next valid edge of SYSREF_x signal after TRIGGER signal reset all the PAWs in the chip
23:20	nco_nu_mode	4'h0000	NCO number mode. 4'b0000 : NCO from reg 4'b10xx : NCO from edge 4'b01xx : NCO from GPIO 4'b1100 : NCO from profile select timer
19:18	reg_nu	2'b00	NCO number from register : choose one of 4 NCO
17	Trig_spi	1'b0	Implement TRIGX pin function with SPI 1 : enable 0 : disable
16	PD_TRIG	1'b1	1 : power down TRIGX pin 0 : power on and TRIGX pin control enable
15:8	Sysref_delay	8'h00	Programable delay on SYSREF path to DDC NCO, 8-bit delay in terms of data clock (single channel mode fs/16 or dual channel mode fs/8)
7:0	Trig_delay	8'h00	Programable delay on TRIGX path to DDC NCO, 8-bit delay in terms of data clock (single channel mode fs/16 or dual channel mode fs/8)

(注意: nco_nu_mode = 4'b1000, NCO from GPIO[0] 0->1 edge 跳变选择 nco_number,一开始为 NCO 0 , 跳变一次加 1， 加到 reg_nu 数值后，再跳变，就回到 0，依此循环。

nco_nu_mode = 4'b1001 NCO from GPIO[1] 0->1 edge 跳变选择 nco_number;

nco_nu_mode = 4'b1010 NCO from GPIO[2] 0->1 edge 跳变选择 nco_number;

nco_nu_mode = 4'b1011 NCO from GPIO[3] 0->1 edge 跳变选择 nco_number;

nco_nu_mode = 4'b0100,通过 GPIO[0]来控制 nco_number 为 0 或者为 1;

nco_nu_mode = 4'b0101,通过 GPIO[1:0]来控制 nco_number 为 0 或者为 1,2,3;

nco_nu_mode = 4'b1100, NCO from PST 计数器选择 nco_number,一开始为 NCO 0 , 累加结束一次加 1， 加到 reg_nu 数值后，再跳变，就回到 0，依此循环。)

DDC PHASE 控制寄存器：only 4 NCO support if single channel mode, set phas0—phase3. in dual channel mode, phase4--phase7 for the second analog input channel

Bits	Name	Default	Descriptions
47:0	{reg168[15:0], reg160[31:0]}	48'd32056872347602	Phase0: 41 degree (41/360) * 2^48
47:0	{reg168[31:16], reg161[31:0]}	48'd32056872347602	Phase1: 41 degree (41/360) * 2^48
47:0	{reg169[15:0], reg162[31:0]}	48'd32056872347602	Phase2: 41 degree (41/360) * 2^48
47:0	{reg169[31:16], reg163[31:0]}	48'd32056872347602	Phase3: 41 degree (41/360) * 2^48
47:0	{reg16a[15:0], reg164[31:0]}	48'd30493122476988	Phase4: 39 degree (39/360) * 2^48
47:0	{reg16a[31:16], reg165[31:0]}	48'd30493122476988	Phase5: 39 degree (39/360) * 2^48
47:0	{reg16b[15:0], reg166[31:0]}	48'd30493122476988	Phase6: 39 degree (39/360) * 2^48
47:0	{reg16b[31:16], reg167[31:0]}	48'd30493122476988	Phase7: 39 degree (39/360) * 2^48

DDC FTW 控制寄存器：only 4 NCO support if single channel mode, set FTW0--FTW3. in dual channel mode, FTW4--FTW7 for the second analog input channel

Bits	Name	Default	Descriptions
47:0	{reg150[15:0], reg16C[31:0]}	48'd136339441844233	FTW0
47:0	{reg150[31:16], reg16D[31:0]}	48'd32985348833280	FTW1
47:0	{reg151[15:0], reg16E[31:0]}	48'd65970697666560	FTW2
47:0	{reg151[31:16], reg16F[31:0]}	48'd136339441844233	FTW3
47:0	{reg156[15:0], reg152[31:0]}	48'd136339441844233	FTW4
47:0	{reg156[31:16], reg153[31:0]}	48'd32985348833280	FTW5
47:0	{reg157[15:0], reg154[31:0]}	48'd67114189759447	FTW6
47:0	{reg157[31:16], reg155[31:0]}	48'd136339441844233	FTW7

DDC 控制寄存器 (地址 9h01 32'h8000_4000)

Bits	Name	Default	Descriptions
31	ddc_soft_rstb	1'b1	Write 0 will reset ddc module
30:28	Uf_window	3'h0	Timing skew Ultra_fine cap steady window value. 0 : 8 1 : 16 2 : 32 3 : 64 4 : 128 5 : 256 6 : 512 7 : 1024
27:25	Adcen_dt	3'h0	Adc_en programmable delay time. 0 : 0us 1 : 100us 2 : 300us 3 : 450us 4 : 600us 5 : 800us 6 : 1ms 7 : 1.5ms
24	Mid_tskew	1'b0	1 : Background timing skew mode0 start from middle value1000_0000 0 : current value
23:18	RVD		
17	Ddc_fs4	1'b0	1/4 Fs IF mode 1 : enable 0 : disable
16	ddc_zif	1'b0	NCO Zero IF , no need NCO and mixer 1 : enable 0 : disable
15:13	ddc_mac_mode	3'b100	DDC MA average number. 0 : 2^14, 1 : 2^15 2 : 2^16 3 : 2^17 4 : 2^18 5 : 2^19 6 : 2^20 7 : 2^21
12	ddc_debug_mode	1'b0	1 : DDC result MA from SPI; 0 ：from MA module
11	ddc_test_mode	1'b0	The input samples are forces to positive full scale and the NCO is enabled. This test mode allows the NCOs to directly drive the decimation filters
10	ddc_gain_6db	1'b0	1 : DDC gain 6dB 0 : DDC gain 0dB
9	ddc_c2r_en	1'b0	DDC Complex to real enable 1 : enable 0 : disable
8	hb1_en	1'b0	DDC Hb1 FIR enable 1 : enable 0 : disable
7	tb2_en	1'b0	DDC Tb2 FIR enable 1 : enable 0 : disable
6	hb2_en	1'b0	DDC Hb2 FIR enable 1 : enable 0 : disable
5	hb3_en	1'b0	DDC Hb3 FIR enable 1 : enable 0 : disable
4	hb4_en	1'b0	DDC Hb4 FIR enable 1 : enable 0 : disable
3	hb5_en	1'b0	DDC Hb5 FIR enable 1 : enable 0 : disable
2	hb6_en	1'b0	DDC Hb6 FIR enable 1 : enable 0 : disable
1	hb7_en	1'b0	DDC Hb7 FIR enable 1 : enable 0 : disable
0	ddcen	1'b0	DDC enable 1 : enable 0 : disable

DDC PST 控制寄存器 （地址 9h1C 32'h0010_0000）

Bits	Name	Default	Descriptions
31:0	PST	32'h0010_0000	profile timer number

JESD204B MAC 寄存器 (地址 7h200-27F)

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x200	version_1	[31:24]	version_1		version number 1	0x20	R
		[23:0]	Reserved		Reserved	0x0	R
0x201	version_2	[31:24]	version_2		version number 2	0x23	R
		[23:0]	Reserved		Reserved	0x0	R
0x202	version_3	[31:24]	version_3		version number 3	0x05	R
		[23:0]	Reserved		Reserved	0x0	R
0x203	version_4	[31:24]	version_4		version number 4	0x31	R
		[23:0]	Reserved		Reserved	0x0	R
0x204	test	[31:24]	test_reg		reg for r/w test.	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x205	global_ctrl	[31]	PMA_pwrdn	0 1	204B IP power down control bit normal work power down	0x0	R/W
		[30:0]	Reserved		Reserved.	0x0	R
0x210	Sync mode	[31:27]	Reserved		Reserved.	0x0	R
		[26:25]	SYSREF± mode select	0 1 10	Disabled. Continuous. One-shot.	0x0	R/W
		[24]	Synchronization mode	0	JESD204B synchronization mode. The SYSREF signal resets all internal clock dividers. Use this mode when synchronizing multiple chips as specified in the JESD204B standard. If the phase of any of the dividers must change, the JESD204B link goes down.	0x0	R/W
				1	Timestamp mode. The SYSREF signal does not reset internal clock dividers. In this mode, the JESD204B link and the signal monitor are not affected by the SYSREF signal. The SYSREF signal timestamps a sample as it passes through the ADC and is used as a control bit in the JESD204B output word.		
		[23:0]	Reserved		Reserved	0x0	R
0x211	sync error report	[31]	sync error cnt clear	0	1: clear error cnt	0x0	R/W
		[30:24]	sync error cnt	0	error cnt	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x212	User Pattern 1 LSB	[31:24]	User Pattern 1 [7:0]		User Test Pattern 1 least significant byte.	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x213	User Pattern 1 MSB	[31:24]	User Pattern 1 [15:8]		User Test Pattern 1 least significant byte.	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x214	User Pattern 2 LSB	[31:24]	User Pattern 2 [7:0]		User Test Pattern 2 least significant byte.	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x215	User Pattern 2 MSB	[31:24]	User Pattern 2 [15:8]		User Test Pattern 2 least significant byte.	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x216	User Pattern 3 LSB	[31:24]	User Pattern 3 [7:0]		User Test Pattern 3 least significant bits.	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x217	User Pattern 3 MSB	[31:24]	User Pattern 3 [15:8]		User Test Pattern 3 least significant bits.	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x218	User Pattern 4 LSB	[31:24]	User Pattern 4 [7:0]		User Test Pattern 4 least significant bits.	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x219	User Pattern 4 MSB	[31:24]	User Pattern 4 [15:8]		User Test Pattern 4 least significant bits.	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x21A	Output Mode Control	[31:31]	Reserved		Reserved.	0x0	R/W
		[29:28]	Converter control Bit 2 selection	0 1 10 11	Tie low (1'b0). control bit0 SYSREF Tie high(1'b1).	0x0	R/W
		[27:26]	Converter control Bit 1 selection	0 1 10 11	Tie low (1'b0). control bit0 SYSREF Tie high(1'b1).	0x0	R/W
		[25:24]	Converter control Bit 0 selection	0 1 10 11	Tie low (1'b0). control bit0 SYSREF Tie high(1'b1).	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x21B	PLL control	[31:28]	JESD204B lane rate control	0000 0001 0010 0011 0100 0101 0110	13.5~17G 8.5~13.5G 6.75~8.5G 4.25~6.75G 3.375~4.25G 2.125~3.375G 1.6875~2.125G	0x0	R/W
		[27:24]	ADC_num	0000 0001 0010	1 adc 2 adc 4 adc	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x21C	PLL status	[31]	clear_loss_lock	0 1	no action clear bit[25]	0x0	R/W
		[30:26]	Reserved	0	Reserved.	0x0	R
		[25]	PLL loss of lock	1	Loss of lock sticky bit. Indicate a loss of lock has occurred at some time. Cleared by setting bit[31].	0x0	R
		[24]	PLL lock status	0 1	Not locked. Locked.	0x0	R
		[23:0]	Reserved		Reserved	0x0	R
0x21D	JESD204B Link status	[31:27]	Reserved		Reserved.	0x0	R
		[26]	sysref_sync_done		received sysref signal	0x0	R
		[25]	link_ready		pma fsm reset done	0x0	R
		[24]	tx_ready		clk_char&clk_samp reset done.	0x0	R
		[23:0]	Reserved		Reserved	0x0	R
0x21E	pdiv/debug_ctrl	[31:28]	Reserved	0000	Reserved.		
		[27:24]	debug_sel		debug pin select control	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x21F	DCM	[31]	Reserved	0	Reserved.		
		[30:24]	DCM	0000000 0000001 0000010 ..... 1111110 1111111	Decimation ratio = 1. Decimation ratio = 2. Decimation ratio = 3. ..... Decimation ratio = 127. Decimation ratio = 128.		
		[23:0]	Reserved		Reserved	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x220	JESD204B Link Control 1	[31]	Standby mode	0 1	Standby mode forces zeros for all converter samples. Standby mode forces code group synchronization (K28.5 characters).	0x0	R/W
		[30]	Tail bit(t) PN	0 1	Disable. Enable.	0x0	R/W
		[29]	Syncb_error_disable	0 1	Subclass 1 or Subclass 2 receiver devices shall indicate the detection of such an error by activating the SYNC~ signal for exactly 2 frame periods. Disable.	0x0	R/W
		[28]	Lane synchronization	0 1	Disable FACI uses /K28.7/. Enable FACI uses /K28.3/ and /K28.7/.	0x1	R/W
		[27:26]	ILAS sequence mode	00 01 11	Initial lane alignment sequence disabled (JESD204B Section 5.3.3.5). Initial lane alignment sequence enabled (JESD204B Section 5.3.3.5). Initial lane alignment sequence always on test mode. JESD204B data link layer test mode where repeated lane alignment sequence (as specified in JESD204B Section 5.3.3.8.2) sent on all lanes.	0x1	R/W
		[25]	FACI	0 1	Frame alignment character insertion enabled (JESD204B Section 5.3.3.4). Frame alignment character insertion disabled. For debug only (JESD204B Section 5.3.3.4).	0x0	R/W
		[24]	Link control	0 1	JESD204B serial transmit link enabled. Transmission of the /K28.5/ characters for code group synchronization is controlled by the SYNC~ signal. JESD204B serial transmit link powered down (held in reset and clock gated).	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x221	JESD204B Link Control 2	[31:30]	SYNCINB± pin control	0 10 11	Normal mode. Ignore SYNCINB± (force CGS). Ignore SYNCINB± (force ILAS/user data).	0x0	R/W
		[29]	SYNCINB± pin invert	0 1	SYNCINB± pin not inverted. SYNCINB± pin inverted.	0x0	R/W
		[28]	Long transport layer test	0 1	JESD204B test samples disabled. JESD204B test samples enabled; long transport layer test sample sequence (as specified in JESD204B Section 5.1.6.3) sent on all link lanes.	0x0	R/W
		[27]	Short transport layer test	0 1	JESD204B test samples disabled. JESD204B test samples enabled; long transport layer test sample sequence (as specified in JESD204B Section 5.1.6.2) sent on all link lanes.	0x0	R/W
		[26]	8-bit/10-bit bypass	0 1	8-bit/10-bit enabled. 8-bit/10-bit bypassed (most significant 2 bits are 0).	0x0	R/W
		[25]	8-bit/10-bit bit invert	0 1	Normal. Invert a, b, c, d, e, f, g, h, I, and j symbols.	0x0	R/W
		[24]	link standby	0 1	Normal mode Link standby mode, clock is on, but only transimit K28.5 code.	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x222	JESD204B Link Control 3	[31:30]	Checksum mode	0 1 10 11	Checksum is the sum of all 8-bit registers in the link configuration table. Checksum is the sum of all individual link configuration fields (LSB aligned). Checksum is disabled (set to zero). For test purposes only. Unused.	0x1	R/W
		[29:28]	Test injection point	0 1 10	N' sample input. 10-bit data at 8-bit/10-bit output (for PHY testing). 8-bit data at scrambler input.	0x0	R/W
		[27:24]	JESD204B test mode patterns	0 1 10 11 100 101 110 111 1000 1110 1111	Normal operation (test mode disabled). Alternating checkerboard. 1/0 word toggle. 31-bit pseudorandom number (PN) sequence: x31 + x28 + 1. 23-bit PN sequence: x23 + x18 + 1. 15-bit PN sequence: x15 + x14 + 1. 9-bit PN sequence: x9 + x5 + 1. 7-bit PN sequence: x7 + x6 + 1. Ramp output. Continuous/repeat user test. Single user test.	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x223	JESD204B Link Control 4	[31:28]	ILAS delay	0	Transmit ILAS on first LMFC after SYNCINB± deasserted.	0x0	R/W
				1	Transmit ILAS on second LMFC after SYNCINB± deasserted.		
				10	Transmit ILAS on third LMFC after SYNCINB± deasserted.		
				11	Transmit ILAS on fourth LMFC after SYNCINB± deasserted.		
				100	Transmit ILAS on fifth LMFC after SYNCINB± deasserted.		
				101	Transmit ILAS on sixth LMFC after SYNCINB± deasserted.		
				110	Transmit ILAS on seventh LMFC after SYNCINB± deasserted.		
				111	Transmit ILAS on eighth LMFC after SYNCINB± deasserted.		
				1000	Transmit ILAS on ninth LMFC after SYNCINB± deasserted.		
				1001	Transmit ILAS on tenth LMFC after SYNCINB± deasserted.		
				1010	Transmit ILAS on eleventh LMFC after SYNCINB± deasserted.		
				1011	Transmit ILAS on twelfth LMFC after SYNCINB± deasserted.		
				1100	Transmit ILAS on thirteenth LMFC after SYNCINB± deasserted.		
				1101	Transmit ILAS on fourteenth LMFC after SYNCINB± deasserted.		
				1110	Transmit ILAS on fifteenth LMFC after SYNCINB± deasserted.		
				1111	Transmit ILAS on sixteenth LMFC after SYNCINB± deasserted.		
		[27]	Reserved		Reserved.	0x0	R
		[26:24]	Link layer test mode	0	Normal operation (link layer test mode disabled).	0x0	R/W
				1	Continuous sequence of /D21.5/ characters.		
				10	Reserved.		
				11	Reserved.		
				100	Modified RPAT test sequence.		
				101	JSPAT test sequence.		
				110	JTSPAT test sequence.		
				111	Reserved.		
		[23:0]	Reserved		Reserved	0x0	R
0x224	JESD204B LMFC offset	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	LMFC phase offset value		Local multiframe clock (LMFC) phase offset value (in frame clocks). Refer to the Deterministic Latency section.	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x225	JESD204B scrambling and number lanes (L) configuration	[31]	JESD204B scrambling (SCR)	0 1	JESD204B scrambler disabled (SCR = 0). JESD204B scrambler enabled (SCR = 1).	0x1	R/W
		[30:29]	Reserved		Reserved.	0x0	R
		[28:24]	JESD204B lanes (L)	0 1 11 … 1111	One lane per link (L = 1). Two lanes per link (L = 2). Four lanes per link (L = 4). Eight lanes per Link (L = 16).	0xB	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x226	JESD204B link number of octets per frames (F)	[31:24]	JESD204B F configuration		JESD204B number of octets per frame (F = JESD204B F configuration + 1) 0 F = 1. 1 F = 2. 10 F = 3. 11 F = 4. 101 F = 6. 111 F = 8. 1111 F = 16.	0x1	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x227	JESD204B link number of frames per multiframe (K)	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	JESD204B K configuration		JESD204B number of frames per multiframe (K = JESD204B K configuration + 1). Only values where F × K is divisible by 4 can be used.	0x1F	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x228	JESD204B link number of converters (M)	[31:24]	JESD204B M configuration		JESD204B number of converters per link/device (M = JESD204B M configuration). 0 Link connected to one virtual converter (M = 1). 1 Link connected to two virtual converters (M = 2). 11 Link connected to four virtual converters (M = 4). 111 Link connected to eight virtual converters (M = 8).	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x229	JESD204B number of control bits (CS) and ADC resolution (N)	[31:31]	Number of control bits (CS) per sample	0 1 10 11	No control bits (CS = 0). 1 control bit (CS = 1), Control Bit 2 only. 2 control bits (CS = 2), Control Bit 2 and Control Bit 1 only. 3 control bits (CS = 3), all control bits (Control Bit 2, Control Bit 1, and Control Bit 0).	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R
		[28:24]	ADC converter resolution (N)	110 111 1000 1001 1010 1011 1100 1101 1110 1111	N = 7-bit resolution. N = 8-bit resolution. N = 9-bit resolution. N = 10-bit resolution. N = 11-bit resolution. N = 12-bit resolution. N = 13-bit resolution. N = 14-bit resolution. N = 15-bit resolution. N = 16-bit resolution.	0xB	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x22A	JESD204B SCV NP configuration	[31:29]	Subclass support	0 1	Subclass 0. Subclass 1.	0x0	R/W
		[28:24]	ADC number of bits per sample(N')	111 1011 1111	N' = 8. N' = 12. N' = 16.	0xB	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x22B	JESD204B JV S configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Samples per converter frame cycle (S)		Samples per converter frame cycle (S = Register 0x0591, Bits[28:24] + 1).	0xF	R
		[23:0]	Reserved		Reserved	0x0	R
0x22C	JESD204B HD CF configuration	[31]	HD value	0 1	High density format disabled. High density format enabled.	0x1	R
		[30:29]	Reserved		Reserved.	0x0	R
		[28:24]	Control words per frame clock cycle per link (CF)		Number of control words per frame clock cycle per link. (CF = 0)	0x0	R
		[23:0]	Reserved		Reserved	0x0	R
0x22D	JESD204B DID configuration	[31:24]	JESD204B Tx DID value		JESD204B serial device identification (DID) number.	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x22E	JESD204B BID configuration	[31:28]	Reserved		Reserved.	0x0	R
		[27:24]	JESD204B Tx BID value		JESD204B serial bank identification (BID) number (extension to DID).	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x230	JESD204B LID0 configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Lane 0 LID value		JESD204B serial lane identification (LID) number for Lane 0.	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x231	JESD204B LID1 configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Lane 1 LID value		JESD204B serial lane identification (LID) number for Lane 1.	0x1	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x232	JESD204B LID2 configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Lane 2 LID value		JESD204B serial lane identification (LID) number for Lane 2.	0x2	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x233	JESD204B LID3 configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Lane 3 LID value		JESD204B serial lane identification (LID) number for Lane 3.	0x3	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x234	JESD204B LID4 configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Lane 4 LID value		JESD204B serial lane identification (LID) number for Lane 4.	0x4	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x235	JESD204B LID5 configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Lane 5 LID value		JESD204B serial lane identification (LID) number for Lane 5.	0x5	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x236	JESD204B LID6 configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Lane 6 LID value		JESD204B serial lane identification (LID) number for Lane 6.	0x6	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x237	JESD204B LID7 configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Lane 7 LID value		JESD204B serial lane identification (LID) number for Lane 7.	0x7	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x238	JESD204B LID8 configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Lane 8 LID value		JESD204B serial lane identification (LID) number for Lane 8.	0x8	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x239	JESD204B LID9 configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Lane 9 LID value		JESD204B serial lane identification (LID) number for Lane 9.	0x9	R/W
		[23:0]	Reserved		Reserved	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x23A	JESD204B LID10 configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Lane 10 LID value		JESD204B serial lane identification (LID) number for Lane 10.	0xA	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x23B	JESD204B LID11 configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Lane 11 LID value		JESD204B serial lane identification (LID) number for Lane 11.	0xB	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x23C	JESD204B LID12 configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Lane 12 LID value		JESD204B serial lane identification (LID) number for Lane 12.	0xC	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x23D	JESD204B LID13 configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Lane 13 LID value		JESD204B serial lane identification (LID) number for Lane 13.	0xD	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x23E	JESD204B LID14 configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Lane 14 LID value		JESD204B serial lane identification (LID) number for Lane 14.	0xE	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x23F	JESD204B LID15 configuration	[31:29]	Reserved		Reserved.	0x0	R
		[28:24]	Lane 15 LID value		JESD204B serial lane identification (LID) number for Lane 15.	0xF	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x240	JESD204B Lane Assign 1	[31:28]	SERDOUT1± lane assignment		Physical Lane 1 assignment.	0x1	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1 (default).		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				x	Logical Lane x.		
				1111	Logical Lane 15.		
		[27:24]	SERDOUT0± lane assignment		Physical Lane 0 assignment.	0x0	R/W
				0	Logical Lane 0 (default).		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				x	Logical Lane x.		
				1111	Logical Lane 15.		
		[23:0]	Reserved		Reserved	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x241	JESD204B Lane Assign 2	[31:28]	SERDOUT3± lane assignment		Physical Lane 3 assignment.	0x3	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3 (default).		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				x	Logical Lane x.		
				1111	Logical Lane 15.		
		[27:24]	SERDOUT2± lane assignment		Physical Lane 2 assignment.	0x2	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1		
				10	Logical Lane 2 (default).		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5.		
				x	Logical Lane x.		
				1111	Logical Lane 15.		
		[23:0]	Reserved		Reserved	0x0	R
0x242	JESD204B Lane Assign 3	[31:28]	SERDOUT5± lane assignment		Physical Lane 5 assignment.	0x5	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				101	Logical Lane 5 (default).		
				x	Logical Lane x.		
				1111	Logical Lane 15.		
		[27:24]	SERDOUT4± lane assignment		Physical Lane 4 assignment.	0x4	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4 (default).		
				101	Logical Lane 5.		
				x	Logical Lane x.		
				1111	Logical Lane 15.		
		[23:0]	Reserved		Reserved	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x243	JESD204B Lane Assign 4	[31:28]	SERDOUT7± lane assignment		Physical Lane 7 assignment.	0x7	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				111	Logical Lane 7 (default).		
				1111	Logical Lane 15.		
		[27:24]	SERDOUT6± lane assignment		Physical Lane 6 assignment.	0x6	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				110	Logical Lane 6 (default).		
				1111	Logical Lane 15.		
		[23:0]	Reserved		Reserved	0x0	R
0x244	JESD204B Lane Assign 5	[31:28]	SERDOUT9± lane assignment		Physical Lane 9 assignment.	0x9	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1001	Logical Lane 9 (default).		
				1111	Logical Lane 15.		
		[27:24]	SERDOUT8± lane assignment		Physical Lane 8 assignment.	0x8	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1000	Logical Lane 8 (default).		
				1111	Logical Lane 15.		
		[23:0]	Reserved		Reserved	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x245	JESD204B Lane Assign 6	[31:28]	SERDOUT11± lane assignment		Physical Lane 11 assignment.	0xB	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1011	Logical Lane 11 (default).		
				1111	Logical Lane 15.		
		[27:24]	SERDOUT10± lane assignment		Physical Lane 10 assignment.	0xA	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1010	Logical Lane 10 (default).		
				1111	Logical Lane 15.		
		[23:0]	Reserved		Reserved	0x0	R
0x246	JESD204B Lane Assign 7	[31:28]	SERDOUT13± lane assignment		Physical Lane 13 assignment.	0xD	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1101	Logical Lane 13 (default).		
				1111	Logical Lane 15.		
		[27:24]	SERDOUT12± lane assignment		Physical Lane 12 assignment.	0xC	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1100	Logical Lane 12 (default).		
				1111	Logical Lane 15.		
		[23:0]	Reserved		Reserved	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x247	JESD204B Lane Assign 7	[31:28]	SERDOUT15± lane assignment		Physical Lane 15 assignment.	0xF	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1110	Logical Lane 14.		
				1111	Logical Lane 15 (default).		
		[27:24]	SERDOUT14± lane assignment		Physical Lane 14 assignment.	0xE	R/W
				0	Logical Lane 0.		
				1	Logical Lane 1.		
				10	Logical Lane 2.		
				11	Logical Lane 3.		
				100	Logical Lane 4.		
				x	Logical Lane x.		
				1110	Logical Lane 14 (default).		
				1111	Logical Lane 15.		
		[23:0]	Reserved		Reserved	0x0	R
0x248	SERDOUTx± data invert	[31]	Invert SERDOUT7± data		Invert SERDOUT7± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[30]	Invert SERDOUT6± data		Invert SERDOUT6± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[29]	Invert SERDOUT5± data		Invert SERDOUT5± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[28]	Invert SERDOUT4± data		Invert SERDOUT4± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[27]	Invert SERDOUT3± data		Invert SERDOUT3± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[26]	Invert SERDOUT2± data		Invert SERDOUT2± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[25]	Invert SERDOUT1± data		Invert SERDOUT1± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[24]	Invert SERDOUT0± data		Invert SERDOUT0± data.	0x0	R/W
				0	Normal.		
				1	Invert.		
		[23:0]	Reserved		Reserved	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x249	SERDOUTx± data invert	[31]	Invert SERDOUT15± data	0 1	Invert SERDOUT15± data. Normal. Invert.	0x0	R/W
		[30]	Invert SERDOUT14± data	0 1	Invert SERDOUT14± data. Normal. Invert.	0x0	R/W
		[29]	Invert SERDOUT13± data	0 1	Invert SERDOUT13± data. Normal. Invert.	0x0	R/W
		[28]	Invert SERDOUT12± data	0 1	Invert SERDOUT12± data. Normal. Invert.	0x0	R/W
		[27]	Invert SERDOUT11± data	0 1	Invert SERDOUT11± data. Normal. Invert.	0x0	R/W
		[26]	Invert SERDOUT10± data	0 1	Invert SERDOUT10± data. Normal. Invert.	0x0	R/W
		[25]	Invert SERDOUT9± data	0 1	Invert SERDOUT9± data. Normal. Invert.	0x0	R/W
		[24]	Invert SERDOUT8± data	0 1	Invert SERDOUT8± data. Normal. Invert.	0x0	R/W
		[23:0]	Reserved		Reserved	0x0	R
0x250	JESD204B Checksum 0 configuration	[31:24]	lane0_chksum		Serial checksum value for Lane 0. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 0) mod 256.		R
		[23:0]	Reserved		Reserved	0x0	R
0x251	JESD204B Checksum 1 configuration	[31:24]	lane1_chksum		Serial checksum value for Lane 1. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 1) mod 256.		R
		[23:0]	Reserved		Reserved	0x0	R
0x252	JESD204B Checksum 2 configuration	[31:24]	lane2_chksum		Serial checksum value for Lane 2. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 2) mod 256.		R
		[23:0]	Reserved		Reserved	0x0	R
0x253	JESD204B Checksum 3 configuration	[31:24]	lane3_chksum		Serial checksum value for Lane 3. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 3) mod 256.		R
		[23:0]	Reserved		Reserved	0x0	R
0x254	JESD204B Checksum 4 configuration	[31:24]	lane4_chksum		Serial checksum value for Lane 4. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 4) mod 256.		R
		[23:0]	Reserved		Reserved	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x255	JESD204B Checksum 5 configuration	[31:24]	lane5_chksum		Serial checksum value for Lane 5. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 5) mod 256.		R
		[23:0]	Reserved		Reserved	0x0	R
0x256	JESD204B Checksum 6 configuration	[31:24]	lane6_chksum		Serial checksum value for Lane 6. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 6) mod 256.		R
		[23:0]	Reserved		Reserved	0x0	R
0x257	JESD204B Checksum 7 configuration	[31:24]	lane7_chksum		Serial checksum value for Lane 7. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 7) mod 256.		R
		[23:0]	Reserved		Reserved	0x0	R
0x258	JESD204B Checksum 8 configuration	[31:24]	lane8_chksum		Serial checksum value for Lane 8. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 8) mod 256.		R
		[23:0]	Reserved		Reserved	0x0	R
0x259	JESD204B Checksum 9 configuration	[31:24]	lane9_chksum		Serial checksum value for Lane 9. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 9) mod 256.		R
		[23:0]	Reserved		Reserved	0x0	R
0x25A	JESD204B Checksum 10 configuration	[31:24]	lane10_chksum		Serial checksum value for Lane 10. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 10) mod 256.		R
		[23:0]	Reserved		Reserved	0x0	R
0x25B	JESD204B Checksum 11 configuration	[31:24]	lane11_chksum		Serial checksum value for Lane 11. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 11) mod 256.		R
		[23:0]	Reserved		Reserved	0x0	R
0x25C	JESD204B Checksum 12 configuration	[31:24]	lane12_chksum		Serial checksum value for Lane 12. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 12) mod 256.		R
		[23:0]	Reserved		Reserved	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x25D	JESD204B Checksum 13 configuration	[31:24]	lane13_chksum		Serial checksum value for Lane 13. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 13) mod 256.		R
		[23:0]	Reserved		Reserved	0x0	R
0x25E	JESD204B Checksum 14 configuration	[31:24]	lane14_chksum		Serial checksum value for Lane 14. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 14) mod 256.		R
		[23:0]	Reserved		Reserved	0x0	R
0x25F	JESD204B Checksum 15 configuration	[31:24]	lane15_chksum		Serial checksum value for Lane 15. Automatically calculated for each lane. Sum (all link configuration parameters for Lane 15) mod 256.		R
		[23:0]	Reserved		Reserved	0x0	R
0x260	PMA fifo wr enable	[31:24]	dbg_fifo_wr[7:0]		fifo wr enable for lane 0~7		R
		[23:0]	Reserved		Reserved	0x0	R
0x261	PMA fifo wr enable	[31:24]	dbg_fifo_wr[15:8]		fifo wr enable for lane 8~15		R
		[23:0]	Reserved		Reserved	0x0	R
0x262	PMA fifo rd enable	[31:24]	dbg_fifo_rd[7:0]		fifo rd enable for lane 0~7		R
		[23:0]	Reserved		Reserved	0x0	R
0x263	PMA fifo rd enable	[31:24]	dbg_fifo_rd[15:8]		fifo rd enable for lane 8~15		R
		[23:0]	Reserved		Reserved	0x0	R
0x264	PMA fifo empty	[31:24]	dbg_fifo_empty[7:0]		fifo empty for lane 0~7		R
		[23:0]	Reserved		Reserved	0x0	R
0x265	PMA fifo empty	[31:24]	dbg_fifo_empty[15:8]		fifo empty for lane 8~15		R
		[23:0]	Reserved		Reserved	0x0	R
0x266	PMA fifo full	[31:24]	dbg_fifo_full[7:0]		fifo full for lane 0~7		R
		[23:0]	Reserved		Reserved	0x0	R
0x267	PMA fifo full	[31:24]	dbg_fifo_full[15:8]		fifo full for lane 8~15		R
		[23:0]	Reserved		Reserved	0x0	R
0x268	PMA ready	[31:24]	dbg_pma_ready[7:0]		pma ready for lane 0~7		R
		[23:0]	Reserved		Reserved	0x0	R
0x269	PMA ready	[31:24]	dbg_pma_ready[15:8]		pm ready for lane 8~15		R
		[23:0]	Reserved		Reserved	0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x26A	PMA fifo rd start	[31:24]	dbg_rd_start[7:0]		fifo rd start for lane 0~7		R
		[23:0]	Reserved		Reserved	0x0	R
0x26B	PMA fifo rd start	[31:24]	dbg_rd_start[15:8]		fifo rd start for lane 8~15		R
		[23:0]	Reserved		Reserved	0x0	R
0x26C	PMA fifo wr start	[31:31]	Reserved		Reserved.		R
		[24]	dbg_wr_start		fifo write start for all lanes		R
		[23:0]	Reserved		Reserved	0x0	R

JESD204B PMA PHY 寄存器 (地址 7h280-2FF)

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x280	pll_cfg0	[31:24]	JESD204B pll cfg0			8'b0111,0101	R/W
		[31:29]	pll_cp_itrim	011	cp current trimming bits 3'b000: 50u 3'b001:100u 3'b010:150u 3'b011:200u default 3'b100:250u 3'b101:300u 3'b110:350u 3'b111:400u		R/W
		[28:27]	pll_cp_rsv	10	cp reset voltage trimming bits 2'b00: (1-12.5%)*vrst voltage 2'b01: (1-6.25%)*vrst voltage 2'b10: vrst voltage default 2'b11: (1+6.25%)*vrst voltage		R/W
		[26:25]	pll_cp_ls	10	cp level shift voltage trimming bits 2'b00: (1+12.5%)*vls voltage 2'b01: vls voltage 2'b10: vls voltage 2'b11: (1+12.5%)*vls voltage		R/W
		[24]	pll_lock_en	1	pll lock detect enable 1'b0: disable 1'b1: enable		R/W
		[23:0]	Reserved			0x0	R
0x281	pll_cfg1	[31:24]	JESD204B pll cfg1			8'b1010,1010	R/W
		[31:29]	pll_lpf_rtrim	101	lpf resistor trimming bits 3'b000: 10k 3'b001: 9k 3'b010: 8k 3'b011: 7k 3'b100: 6k 3'b101: 5k default 3'b110: 4k 3'b111: 3k		R/W
		[28:27]	pll_div2_itrim	01	high speed div2 current trimming bits 2'b00: 1.6mA 2'b01: 2mA 2'b10: 2.4mA 2'b11: 2.8mA		R/W
		[26:25]	pll_div2_buf	01	high speed div2buf current trimming bits 2'b00: 2mA 2'b01: 3mA 2'b10: 3mA 2'b11: 4mA		R/W
		[24]	RSV	0	Reserved		R/W
		[23:0]	Reserved			0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x282	pll_cfg2	[31:24]	JESD204B pll cfg2			8'b0100,0010	R/W
		[31]	pll_vco_rtrim_mannul	0	pll vco rtrim mannul trimming bit 1'b0: auto mode 1'b1: mannul mode		
		[30:26]	pll_vco_rtrim_reg	10000	pll vco rtrim code in mannul mode		
		[25:24]	pll_fbdiv<1:0>	10	pll feedback divider ratio trimming bits 2'b00: /16 2'b01: /32 2'b10: /20 default 2'b11: /40		
		[23:0]	Reserved			0x0	R
0x283	pll_cfg3	[31:24]	JESD204B pll cfg3			8'b0001,0100	R/W
		[31]	pll_tsten	0	pll test enable 1'b0: disable 1'b1: enable		
		[30:29]	pll_atest_sel	00	pll analog voltage select 2'b00: no select 2'b01: select ldo voltage output 2'b10: select vcntl voltage output		
		[28:27]	pll_lock_factor	10	pll lock detect frequency compare mask select 2'b00:16'b1111 1111 1111 1000 2'b01:16'b1111 1111 1111 0000 2'b10:16'b1111 1111 1110 0000 default 2'b11:16'b1111 1111 1100 0000		
		[26:25]	pll_lock_coarse	10	pll lock detect frequency compare counter select 2'b00:16'd65535 2'b01:16'd4095 2'b10:16'd1023 default 2'b11:16'd255		
		[24]	RSV	0	Reserved		
		[23:0]	Reserved			0x0	R
0x284	pll_cfg4	[31:24]	JESD204B pll cfg4			8'b0100,0001	R/W
		[31]	pll_vco_crs_ovrden	0	vco code overwrite enable 1'0： disable 1'b1: enable		
		[30:25]	pll_vco_code	100000	vco overwrite code, mannul mode		
		[24]	pll_vco_ofst_en	1	ignore vco code offset enable 1'b0: disable, vco code with offset 1'b1: enable, ignore offset		
		[23:0]	Reserved			0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x285	pll_cfg5	[31:24]	JESD204B pll cfg5			8'0001,1001	R/W
		[31]	pll_vco_band_sel	0	vco high band and low band select in mannul mode 1'b0：select high band 1'b1: select low band		
		[30:29]	pll_vco_accuracy	00	vco calibration perilod select 2b'00: 4095 default 2b'01: 1023 2b'10: 16383 2b'11: 65535		
		[28]	pll_vco_band_sel_auto	1	auto select vco high band and low band 1'b0：mannul mode 1'b1: auto mode		
		[27:26]	pll_vco_offset	10	offset of the vco coarse tuning code setting 2b'00: -1 2b'01: -2 2b'10: +1 2b'11: +2		
		[25:24]	pll_lock_latency_sel	01	waiting time trimming when pll in the closed loop pll 2b'00: 65535 2b'01: 16383 default 2b'10: 4095 2b'11: 1023		
		[23:0]	Reserved	0x0	R	[23:0]	Reserved
0x286	rcal_cfg0	[31:24]	JESD204B rcal cfg0			8'b0101,0110	R/W
		[31:30]	ircal50u_cal_ctl	01	current trimming for the resistor calibration block 2'b00:1mA*98% 2'b01:1mA 2'b10:1mA*1.02% 2'b11:1mA*1.04%		
		[29:28]	ircal50u_pll_ctl	01	pll calibration current trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[27:26]	ircal50u_tx_ctl	01	tx calibration current trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[25]	rcalenb_manual	1	resistor calibration mode 1’b0: manual mode 1‘b1:auto mode		
		[24]	iref_testen	0	test enable for accurate 50u current for adc core 1'b0: disable 1'b1: enable		
		[23:0]	Reserved			0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x287	rcal_cfg1	[31:24]	JESD204B rcal cfg1			8'b0000,0000	R/W
		[31:29]	txcal_offset	000	tx cailibration code offset 3'b000: rcal _tx[4:0]= rcal[4:0] 3'b001: rcal _tx[4:0]= rcal[4:0]+1 3'b010: rcal _tx[4:0]= rcal[4:0]+2 3'b011: rcal _tx[4:0]= rcal[4:0]+3 3'b100: rcal _tx[4:0]= rcal[4:0] 3'b101: rcal _tx[4:0]= rcal[4:0]-1 3'b110: rcal _tx[4:0]= rcal[4:0]-2 3'b111: rcal _tx[4:0]= rcal[4:0]-3		
		[28:26]	pllcal_offset	000	pll calibration code offset 3'b000: rcal _pll[4:0]= rcal[4:0] 3'b001: rcal _pll[4:0]= rcal[4:0]+1 3'b010: rcal _pll[4:0]= rcal[4:0]+2 3'b011: rcal _pll[4:0]= rcal[4:0]+3 3'b100: rcal _pll[4:0]= rcal[4:0] 3'b101: rcal _pll[4:0]= rcal[4:0]-1 3'b110: rcal _pll[4:0]= rcal[4:0]-2 3'b111: rcal _pll[4:0]= rcal[4:0]-3		
		[25:24]	RSV	00	Reserved		
		[23:0]	Reserved			0x0	R
0x288	tx_cfg0	[31:24]	JESD204B tx cfg0			8'b1110,0000	R/W
		[31:30]	tx_wide_mode, tx_divbyfive	11	tx data width select 2'b00: 16 bits 2'b01: 20 bits 2'b10: 32 bits 2'b11: 40 bits		
		[29:27]	tx_drvbiastrim	100	driver bias current trimming 3'b000: -40uA 3'b001: -30uA 3'b010: -20uA 3'b011: -10uA 3'b100: +0uA 3'b101: +10uA 3'b110: +20uA 3'b111: +30uA		
		[26:24]	tx_emppre	000	tx pre-cursor setting		
		[23:0]	Reserved			0x0	R
0x289	tx_cfg1	[7:0]	JESD204B tx cfg1			8'b1000,0000	R/W
		[7:3]	tx_termprog	10000	tx code manual		
		[2]	tx_dcc_enb	0	tx duty cycle calibration enable, active low 1'b0: enable 1'b1: disable		
		[1]	tx_termcodesel	0	tx code mode select 1'b0: auto mode 1'b1: manual mode		
		[0]	tx_termtest	0	tx term test		
		[23:0]	Reserved			0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x28A	tx_cfg2	[7:0]	JESD204B tx cfg2			8'b0000,0000	R/W
		[7]	tx_tstdiven	0	tx low speed data test enable 1'b0: disable 1'b1: enable		
		[6:3]	tx_amonsel	0000	tx analog test voltage select, detail see TestMux		
		[2]	tx_pdivsel<2>	0	tx post divider by 16 when it is enabled		
		[1]	tx_prbs_en	0	tx prbs enable 1'b0:disable 1'b1: enable		
		[0]	tx_prbs_mode	0	tx prbs mode select 1'b0: 0101 pattern 1'b1: prbs7 pattern		
		[23:0]	Reserved			0x0	R
0x28B	com_cfg0	[7:0]	JESD204B com cfg0			8'b0000,0000	R/W
		[7]	RSV	0	Reserved		
		[6]	com_dig_tst_sel	0	digital signal select 1'b0: select refclk for com_tstclk<0> /select fbclk for com_tstclk<1> 1'b1: select tielow for com_tstclk<0> /select cfgclk for com_tstclk<1>		
		[5:0]	com_ana_tst_sel	000000	analog signal select detail see TestMux		
		[23:0]	Reserved			0x0	R
0x28C	bg_cfg0	[7:0]	JESD204B bg cfg0			8'b0101,0101	R/W
		[7:6]	ir50u_pll_ctrl	01	vbg/r current of pll trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[5:4]	ir50u_buff_ctrl	01	vbg/r current of buffer trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[3:2]	ir50u_rcal_ctrl	01	vbg/r current of rcal trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[1:0]	ir50u_spare_ctrl	01	vbg/r current of spare trimming bits for 50u 2'b00:45u 2'b01:50u 2'b10:55u 2'b11:60u		
		[23:0]	Reserved			0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x28D	bg_cfg1	[31:24]	JESD204B bg cfg1			8'b0110,0000	R/W
		[31:30]	bg_trimcom	01	vbg voltage trimming bits 2'b00:1.193v 2'b01:1.216v 2'b10:1.24v 2'b11:1.264v		
		[29:27]	bg_trimvco	100	vco voltage trimming bits 3'b000:1.119v 3'b001:1.144v 3'b010:1.168v 3'b011:1.193v 3'b100:1.216v 3'b101:1.24v 3'b110:1.264v 3'b111:1.288v		
		[26]	bg_safemode	0	bg safe mode enable 1'b0: normal mode 1'b1: safe mode		
		[25]	bg_testen	0	bg test enable 1'b0: disable 1'b1: enable		
		[24]	RSV	0	Reserved		
		[23:0]	Reserved			0x0	R
0x28E	pma_top_cfg0	[31:24]	JESD204B pma top cfg0			8'b1000,0000	R/W
		[31:30]	pma_top_buf_itrim	10	clock buffer trimming bits 2'b00: 2mA 2'b01: 3mA 2'b10: 3mA 2'b11: 4mA		
		[29]	RSV	0	Reserved		
		[28:24]	pma_top_clktst_sel	00000	pma top test signal select detail see TestMux		
		[23:0]	Reserved			0x0	R
0x28F	pma_top_cfg1	[31:24]	JESD204B pma top cfg1			8'b0000,0001	R/W
		[31]	bg_pwrdn	0	bg power down enable 1'b0: normal work 1'b1: power down	.	
		[30]	pll_pwrdn	0	pll power down enable 1'b0: normal work 1'b1: power down		
		[29:28]	RSV	000000	Reserved		
		[27]	pllck_dccfix	0	pllck duty cycle calibration fixed function 1'b0: normal work 1'b1: dcc output fixed to an equal level		
		[26]	pllck_dccenb	0	pllck duty cycle calibration enable, active low 1'b0: normal work 1'b1: disable pllck dcc funciton		
		[25:24]	pllck_dcctrim	01	dcc current trimming bits 2'b00: 0.6mA 2'b01: 0.9mA 2'b10: 1.2mA 2'b11: 1.5mA		
		[23:0]	Reserved			0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x290	adc_clk_stime	[31:24]	JESD204B adc clk wait time			8'b1000,0000	R/W
		[31:27]	cfg_clk_wait_time	10000	PMA reset sequence adc_clk stable time control bits: cycle = 2^adc_clk_stime 5'b00000: 1 cycles of Cfg_Clk; 5'b00001: 2^1 cycles of Cfg_Clk; 5'b00010: 2^2 cycles of Cfg_Clk; ….; 5'b10000: 2^16 cycles of Cfg_Clk; default ….; 5'b11111: 2^31 cycles of Cfg_Clk;		
		[26:24]	RSV	000	Reserved		
		[23:24]	Reserved			0x0	R
0x291	fsm_reset_seq	[31:24]	JESD204B fsm reset			8'b0000,0000	R/W
		[31]	top_seq_bypass	0	top sequence bypass 1'b0: normal work 1'b1: bypass		
		[30]	lnk_rdy	0	link_ready 1'b0: not ready 1'b1: link ready		
		[29]	rcal_enb	0	rcal enable,active low 1'b0: enable 1'b1: disable		
		[28]	pll_rstb	0	pll reset,active low 1'b0: reset 1'b1: normal work		
		[27]	tx_rstb	0	tx reset,active low 1'b0: reset 1'b1: normal work		
		[26]	rstb_d	0	mac reset,active low 1'b0: reset 1'b1: normal work		
		[25:24]	RSV	00	Reserved		
		[23:0]	Reserved			0x0	R
0x292	divider_cfg	[31:24]	JESD204B divider cfg in mannual			8'b0000,0000	R/W
		[31:30]	pll_mdiv	00	mdivider select config in mannual 2'b00: /1 2'b01: /2 2'b10: /4 2'b11: /8		
		[29:28]	tx_pdiv	00	pdivide select config in mannual 2'b00: /1 2'b01: /2 2'b10: /4 2'b11: /8		
		[27]	div_sel	0	1'b0: pll_mdiv/tx_pdiv use fsm value 1'b1: pll_mdiv/tx_pdiv use reg 0x12 bits [31:28].		
		[26]	adcdiv1	0	predivider in adc. 0: div 2 1: div 3		
		[25:24]	adcdiv0	00	predivider in adc. 00: div 1 01: div 2 10: div 4 11: div 8		
		[23:0]	Reserved			0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x293	time_1us_set	[31:24]	time count for 1us			8'b1000,1010	R/W
		[31:24]	time_1us	1000,1010	timer count for 1.25us at 110MHz		
		[23:0]	Reserved			0x0	R
0x294	tx_pwr_cfg0	[31:24]	tx power down config			8'b0000,0000	R/W
		[31:24]	tx_pwrdn	0000,0000	tx power down 1'b0: normal work 1'b1: power down bit<7>: control lane7 ... bit<0>: control lane0		
		[23:0]	Reserved			0x0	R
0x295	tx_pwr_cfg1	[31:24]	tx power down config			8'b0000,0000	R/W
		[31:24]	tx_pwrdn	0000,0000	tx power down 1'b0: normal work 1'b1: power down bit<7>: control lane15 ... bit<0>: control lane8		
		[23:0]	Reserved			0x0	R
0x296	pll_status	[31:24]	pll status			8'b0000,0000	R
		[31]	RSV	0	Reserved		
		[30]	pll_afc_fine_en		pll fine tuning mode indicator 1'b0: coarse tuning process 1'b1: fine tuning process		
		[29:24]	pll_vco_ctrim		vco band code		
		[23:0]	Reserved			0x0	R
0x297	rcal_code	[31:24]	rcal code			8'b0000,0000	R
		[31:29]	RSV	00	Reserved		
		[28:24]	rcal_code		resistor calibration code		
		[23:0]	Reserved			0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2A0	tx_drvamp_cfg0	[31:24]	tx drvamp cfg0			8'b0100,0100	R/W
		[31]	RSV	0	Reserved		
		[30:28]	tx_drvamp_lane1	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[27]	RSV	0	Reserved		
		[26:24]	tx_drvamp_lane0	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[23:0]	Reserved			0x0	R
0x2A1	tx_drvamp_cfg1	[31:24]	tx drvamp cfg1			8'b0100,0100	R/W
		[31]	RSV	0	Reserved		
		[30:28]	tx_drvamp_lane3	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[27]	RSV	0	Reserved		
		[26:24]	tx_drvamp_lane2	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[23:0]	Reserved			0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2A2	tx_drvamp_cfg2	[31:24]	tx drvamp cfg2			8'b0100,0100	R/W
		[31]	RSV	0	Reserved		
		[30:28]	tx_drvamp_lane5	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[27]	RSV	0	Reserved		
		[26:24]	tx_drvamp_lane4	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[23:0]	Reserved			0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2A3	tx_drvamp_cfg3	[31:24]	tx drvamp cfg3			8'b0100,0100	R/W
		[31]	RSV	0	Reserved		
		[30:28]	tx_drvamp_lane7	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[27]	RSV	0	Reserved		
		[26:24]	tx_drvamp_lane6	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[23:0]	Reserved			0x0	R
0x2A4	tx_drvamp_cfg4	[31:24]	tx drvamp cfg4			8'b0100,0100	R/W
		[31]	RSV	0	Reserved		
		[30:28]	tx_drvamp_lane9	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[27]	RSV	0	Reserved		
		[26:24]	tx_drvamp_lane8	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[23:0]	Reserved			0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2A5	tx_drvamp_cfg5	[31:24]	tx drvamp cfg5			8'b0100,0100	R/W
		[31]	RSV	0	Reserved		
		[30:28]	tx_drvamp_lane11	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[27]	RSV	0	Reserved		
		[26:24]	tx_drvamp_lane10	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[23:0]	Reserved			0x0	R
0x2A6	tx_drvamp_cfg6	[31:24]	tx drvamp cfg6			8'b0100,0100	R/W
		[31]	RSV	0	Reserved		
		[30:28]	tx_drvamp_lane13	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[27]	RSV	0	Reserved		
		[26:24]	tx_drvamp_lane12	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[23:0]	Reserved			0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2A7	tx_drvamp_cfg7	[31:24]	tx drvamp cfg7			8'b0100,0100	R/W
		[31]	RSV	0	Reserved		
		[30:28]	tx_drvamp_lane15	100	tx driver output amplitude control bits for lane1 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[27]	RSV	0	Reserved		
		[26:24]	tx_drvamp_lane14	100	tx driver output amplitude control bits for lane0 3'b000 = 326 mV p-p, 3'b001 = 405 mV p-p, 3'b010 = 483 mV p-p, 3'b011 = 560 mV p-p, 3'b100 = 634 mV p-p, default 3'b101 = 704 mV p-p, 3'b110 = 768 mV p-p, 3'b111 reserved		
		[23:0]	Reserved			0x0	R
0x2A8	tx_post_tap_cfg0	[31:24]	tx post tap cfg0			8'b0000,0000	R/W
		[31]	RSV	0	Reserved		
		[30:28]	tx_post_tap_lane1	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[27]	RSV	0	Reserved		
		[26:24]	tx_post_tap_lane0	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[23:0]	Reserved			0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2A9	tx_post_tap_cfg1	[31:24]	tx post tap cfg1			8'b0000,0000	R/W
		[31]	RSV	0	Reserved		
		[30:28]	tx_post_tap_lane3	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[27]	RSV	0	Reserved		
		[26:24]	tx_post_tap_lane2	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[23:0]	Reserved			0x0	R
0x2AA	tx_post_tap_cfg2	[31:24]	tx post tap cfg2			8'b0000,0000	R/W
		[31]	RSV	0	Reserved		
		[30:28]	tx_post_tap_lane5	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[27]	RSV	0	Reserved		
		[26:24]	tx_post_tap_lane4	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[23:0]	Reserved			0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2AB	tx_post_tap_cfg3	[31:24]	tx post tap cfg3			8'b0000,0000	R/W
		[31]	RSV	0	Reserved		
		[30:28]	tx_post_tap_lane7	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[27]	RSV	0	Reserved		
		[26:24]	tx_post_tap_lane6	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[23:0]	Reserved			0x0	R
0x2AC	tx_post_tap_cfg4	[31:24]	tx post tap cfg4			8'b0000,0000	R/W
		[31]	RSV	0	Reserved		
		[30:28]	tx_post_tap_lane9	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[27]	RSV	0	Reserved		
		[26:24]	tx_post_tap_lane8	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[23:0]	Reserved			0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2AD	tx_post_tap_cfg5	[31:24]	tx post tap cfg5			8'b0000,0000	R/W
		[31]	RSV	0	Reserved		
		[30:28]	tx_post_tap_lane11	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[27]	RSV	0	Reserved		
		[26:24]	tx_post_tap_lane10	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[23:0]	Reserved			0x0	R
0x2AE	tx_post_tap_cfg6	[31:24]	tx post tap cfg6			8'b0000,0000	R/W
		[31]	RSV	0	Reserved		
		[30:28]	tx_post_tap_lane13	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[27]	RSV	0	Reserved		
		[26:24]	tx_post_tap_lane12	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[23:0]	Reserved			0x0	R

Addr_ example	Name	Bits	Bit Name	Settings	Description	Reset	Access
0x2AF	tx_post_tap_cfg7	[31:24]	tx post tap cfg7			8'b0000,0000	R/W
		[31]	RSV	0	Reserved		
		[30:28]	tx_post_tap_lane15	000	tx post tap level control for lane1 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[27]	RSV	0	Reserved		
		[26:24]	tx_post_tap_lane14	000	tx post tap level control for lane0 3'b000 = 0 dB 3'b001 = 1.1dB, 3'b010 = 2.4dB, 3'b011 = 3.9dB, 3'b100 = 5.8dB, 3'b101 = 8.2dB, 3'b110 = 11.5dB, 3'b111 reserved		
		[23:0]	Reserved			0x0	R

10 使用说明(Application Information)

10.1 初始化设置(Initialization Set Up)

ADC 和 JESD204B 接口需要进行初始化配置来进入工作状态，配置流程可以参考以下：

1. 芯片上电
2. 根据采样率提供相应频率的时钟
3. 等待时钟稳定至少 500ms
4. 配置 Dual_mode (寄存器 0x005 的[18])，配置 0 切换到单通道模式，配置 1 切换到双通道模式
5. 配置 PD18_BUF 为 1
6. 配置 JESD204B 接口相关参数
   (1) 配置 SYSREF MODE(寄存器 0x210)，暂时停用 SYSREF
   (2) 配置 JESD204B lane rate control 和 ADC_num (寄存器 0x21B)
   (3) 配置 DCM (寄存器 0x21F)
   (4) 配置 JESD204 scrambling configuration 和 JESD204B L configuration (寄存器 0x225)
   (5) 配置 JESD204B F configuration (寄存器 0x226)
   (6) 配置 JESD204B M configuration (寄存器 0x228)
   (7) 配置 JESD204B CS configuration 和 ADC converter resolution (寄存器 0x229)
   (8) 配置 JESD204B Subclass configuration (暂时配置为子类 0) 和 N' configuration (寄存器 0x22A)
   (9) 配置 JESD204B S configuration (寄存器 0x22B)
   (10) 根据 PCB 连接关系配置 Serdes 的 Lane Assignment 和 polarity invert (寄存器 0x240-0x249)
7. 配置 PD_SYSREF (寄存器 0x004 的[9])为 1，再配置 PD_SYSREF 为 0，使能芯片 SYSREF 管脚
8. 配置时钟芯片发送单个 SYSREF 脉冲给 ADC
9. 通过芯片 RESET_ANALOG 管脚提供 1.8V 的复位脉冲信号，让 ADC 内部进行对齐
10. 配置时钟芯片发送单个 SYSREF 脉冲给 ADC
11. 配置 SYSREF MODE 为 one-shot 模式 (0b10), SUBCLASS 配置为子类 1。
12. 配置 ADC_EN (寄存器 0x101 的[11])为 0，然后配置 ADC_EN 为 1，对 ADC 进行软复位
13. 配置时钟芯片发送单个 SYSREF 脉冲给 ADC
14. 软复位 RX，进行建链
15. 配置时钟芯片发送单个 SYSREF 脉冲给 FPGA
16. 可以通过 ILA 等工具监测链路的 SYNC 信号看是否稳定，如果观测到 SYNC 有突然拉低的抖动，且都发生在多帧边界 (Xilinx JESD IP 的 start_of_multiframe = 1)，此时 ADC 时钟和 SYSREF 的相位关系有 setup/hold 违例，需要调整时钟芯片 SYSREF 输出的延时。后续每次上电都保证相同的相位关系，可以稳定避开 setup/hold 违例
17. 配置 PD18_BUF 为 0

10.2 切换单通道/双通道模式

芯片上电后，默认是单通道模式，可以按以下流程切换单通道/双通道模式：

1. 配置 Dual_mode (寄存器 0x005 的[18])，配置 0 切换到单通道模式，配置 1 切换到双通道模式
2. 配置寄存器 0x1C 为 0x00100000
3. 通过芯片 RESET_ANALOG 管脚提供 1.8V 的复位脉冲信号，让 ADC 内部进行对齐
4. 配置 ADC_EN (寄存器 0x101 的[11])为 0，然后配置 ADC_EN 为 1，对 ADC 进行软复位

10.3 JESD204B 数据映射

JESD204B 接口将 ADC 数据进行映射，经过 8B/10B 编码后发送到接收端。
不同模式使用的参数可以查阅下表。

	F	M	L	S	N'	N	HD	ADC_num
16lane 单通道模式	2	1	16	16	16	12	0	1
12lane 单通道模式	2	1	12	16	12	12	1	1
6lane 单通道模式	2	1	6	8	12	12	1	1
16lane 双通道模式	2	2	16	8	16	12	0	2
12lane 双通道模式	2	2	12	8	12	12	1	2
6lane 双通道模式	2	2	6	4	12	12	1	2

16Lane 单通道模式映射

LANE	Frame 0			
	Octet0		Octet1	
	Nibble 0	Nibble 1	Nibble 2	Nibble 3
DA0	S0[11:0]			4'B0000
DA1	S1[11:0]			4'B0000
DA2	S2[11:0]			4'B0000
DA3	S3[11:0]			4'B0000
DA4	S4[11:0]			4'B0000
DA5	S5[11:0]			4'B0000
DA6	S6[11:0]			4'B0000
DA7	S7[11:0]			4'B0000
DB0	S8[11:0]			4'B0000
DB1	S9[11:0]			4'B0000
DB2	S10[11:0]			4'B0000
DB3	S11[11:0]			4'B0000
DB4	S12[11:0]			4'B0000
DB5	S13[11:0]			4'B0000
DB6	S14[11:0]			4'B0000
DB7	S15[11:0]			4'B0000

12Lane 单通道模式映射

LANE	Frame 0			
	Octet0		Octet1	
	Nibble 0	Nibble 1	Nibble 2	Nibble 3
DA0	S0[11:0]			S1[11:8]
DA1	S1[7:0]		S2[11:4]	
DA2	S2[3:0]	S3[11:0]		
DA3	S4[11:0]			S5[11:8]
DA4	S5[7:0]		S6[11:4]	
DA5	S6[3:0]	S7[11:0]		
DA6	S8[11:0]			S9[11:8]
DA7	S9[7:0]		S10[11:4]	
DB0	S10[3:0]	S11[11:0]		
DB1	S12[11:0]			S13[11:8]
DB2	S13[7:0]		S14[11:4]	
DB3	S14[3:0]	S15[11:0]		
DB4	not used			
DB5				
DB6				
DB7				

6Lane 双通道模式映射

LANE	Frame 0			
	Octet0		Octet1	
	Nibble 0	Nibble 1	Nibble 2	Nibble 3
DA0	S0[11:0]			S1[11:8]
DA1	S1[7:0]		S2[11:4]	
DA2	S2[3:0]	S3[11:0]		
DA3	S4[11:0]			S5[11:8]
DA4	S5[7:0]		S6[11:4]	
DA5	S6[3:0]	S7[11:0]		
DA6	not used			
DA7				
DB0				
DB1				
DB2				
DB3				
DB4				
DB5				
DB6				
DB7				

16Lane 双通道模式映射

LANE	Frame 0			
	Octet0		Octet1	
	Nibble 0	Nibble 1	Nibble 2	Nibble 3
DA0	M0S0[11:0]			4'B0000
DA1	M0S1[11:0]			4'B0000
DA2	M0S2[11:0]			4'B0000
DA3	M0S3[11:0]			4'B0000
DA4	M0S4[11:0]			4'B0000
DA5	M0S5[11:0]			4'B0000
DA6	M0S6[11:0]			4'B0000
DA7	M0S7[11:0]			4'B0000
DB0	M1S0[11:0]			4'B0000
DB1	M1S1[11:0]			4'B0000
DB2	M1S2[11:0]			4'B0000
DB3	M1S3[11:0]			4'B0000
DB4	M1S4[11:0]			4'B0000
DB5	M1S5[11:0]			4'B0000
DB6	M1S6[11:0]			4'B0000
DB7	M1S7[11:0]			4'B0000

12Lane 双通道模式映射

LANE	Frame 0			
	Octet0		Octet1	
	Nibble 0	Nibble 1	Nibble 2	Nibble 3
DA0	M0S0[11:0]			M0S1[11:8]
DA1	M0S1[7:0]		M0S2[11:4]	
DA2	M0S2[3:0]	M0S3[11:0]		
DA3	M0S4[11:0]			M0S5[11:8]
DA4	M0S5[7:0]		M0S6[11:4]	
DA5	M0S6[3:0]	M0S7[11:0]		
DA6	M1S0[11:0]			M1S1[11:8]
DA7	M1S1[7:0]		M1S2[11:4]	
DB0	M1S2[3:0]	M1S3[11:0]		
DB1	M1S4[11:0]			M1S5[11:8]
DB2	M1S5[7:0]		M1S6[11:4]	
DB3	M1S6[3:0]	M1S7[11:0]		
DB4	not used			
DB5				
DB6				
DB7				

6Lane 双通道模式映射

LANE	Frame 0			
	Octet0		Octet1	
	Nibble 0	Nibble 1	Nibble 2	Nibble 3
DA0	M0S0[11:0]			M0S1[11:8]
DA1	M0S1[7:0]		M0S2[11:4]	
DA2	M0S2[3:0]	M0S3[11:0]		
DA3	M1S0[11:0]			M1S1[11:8]
DA4	M1S1[7:0]		M1S2[11:4]	
DA5	M1S2[3:0]	M1S3[11:0]		
DA6	not used			
DA7				
DB0				
DB1				
DB2				
DB3				
DB4				
DB5				
DB6				
DB7				

11 封装尺寸 (Package Outline)

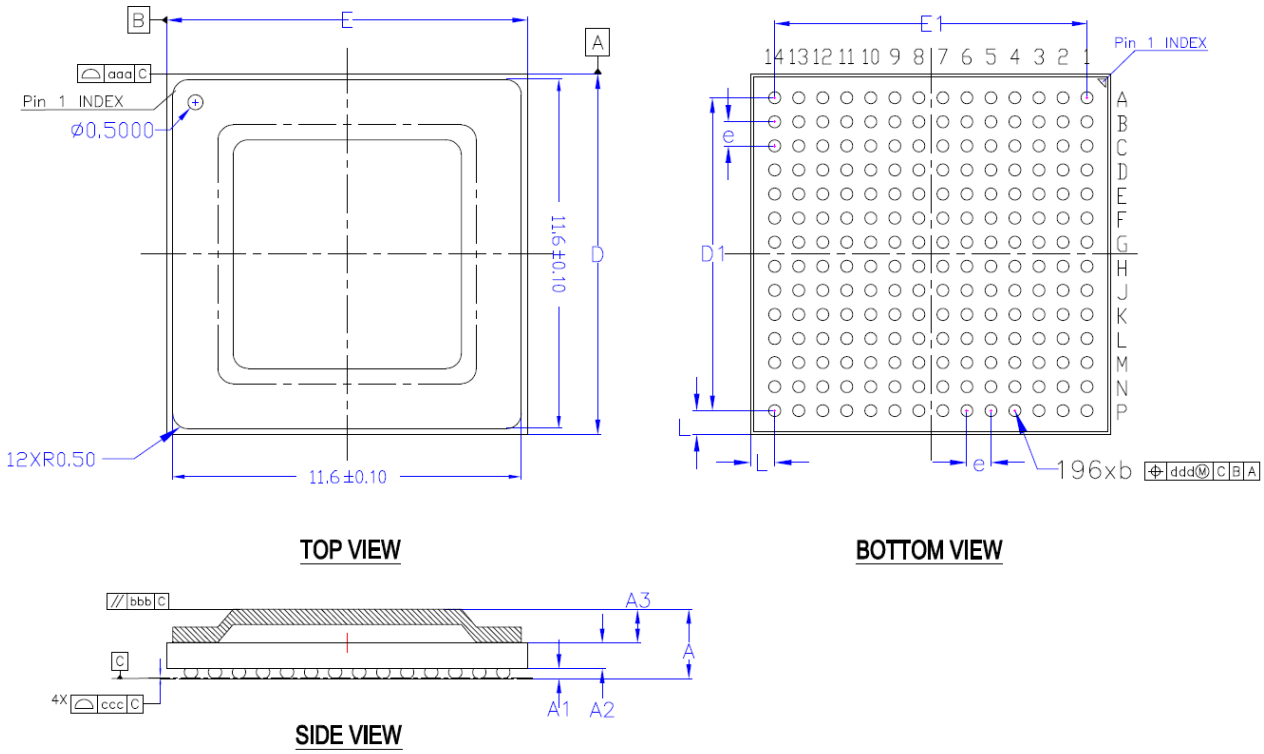


图 11-1. FCBGA196 封装尺寸图

Dimensional Ref.

REF. Min.		Nom.	Max.
A	2.13	2.32	2.51
A1	0.30	0.35	0.40
A2	0.76	0.85	0.94
A3	1.07	1.12	1.17
D	11.9	12.0	12.1
E	11.9	12.0	12.1
D1	10.4 BSC		
E1	10.4 BSC		
L	0.8 REF		
e	0.8 BSC		
b	0.40	0.45	0.50
Tol. of Form & Position			
aaa	0.10		
bbb	0.10		
ccc	0.20		
ddd	0.05		

Notes:

1. All Dimensions are in Millimeters (Angles in Degrees).
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

12 订购指南 (Orderable Information)

型号	产品描述	温度范围	封装描述	封装选项
CAE2400	12 位 6Gsps 射频采样 ADC	-40℃ 至 +115℃	196 球- 倒装球栅阵列封装	FCBGA-196

重要声明和免责声明

Caelus“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 Caelus产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的Caelus 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。Caelus授权您仅可将这些资源用于研发本资源所述的Caelus 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 Caelus 知识产权或任何第三方知识产权。

Caelus提供的产品受 Caelus 的销售条款或Caelus产品随附的其他适用条款的约束。Caelus提供这些资源并不会扩展或以其他方式更改Caelus针对 Caelus产品发布的适用的担保或担保免责声明。

Copyright © 2024，奇历士 (Caelus) 公司